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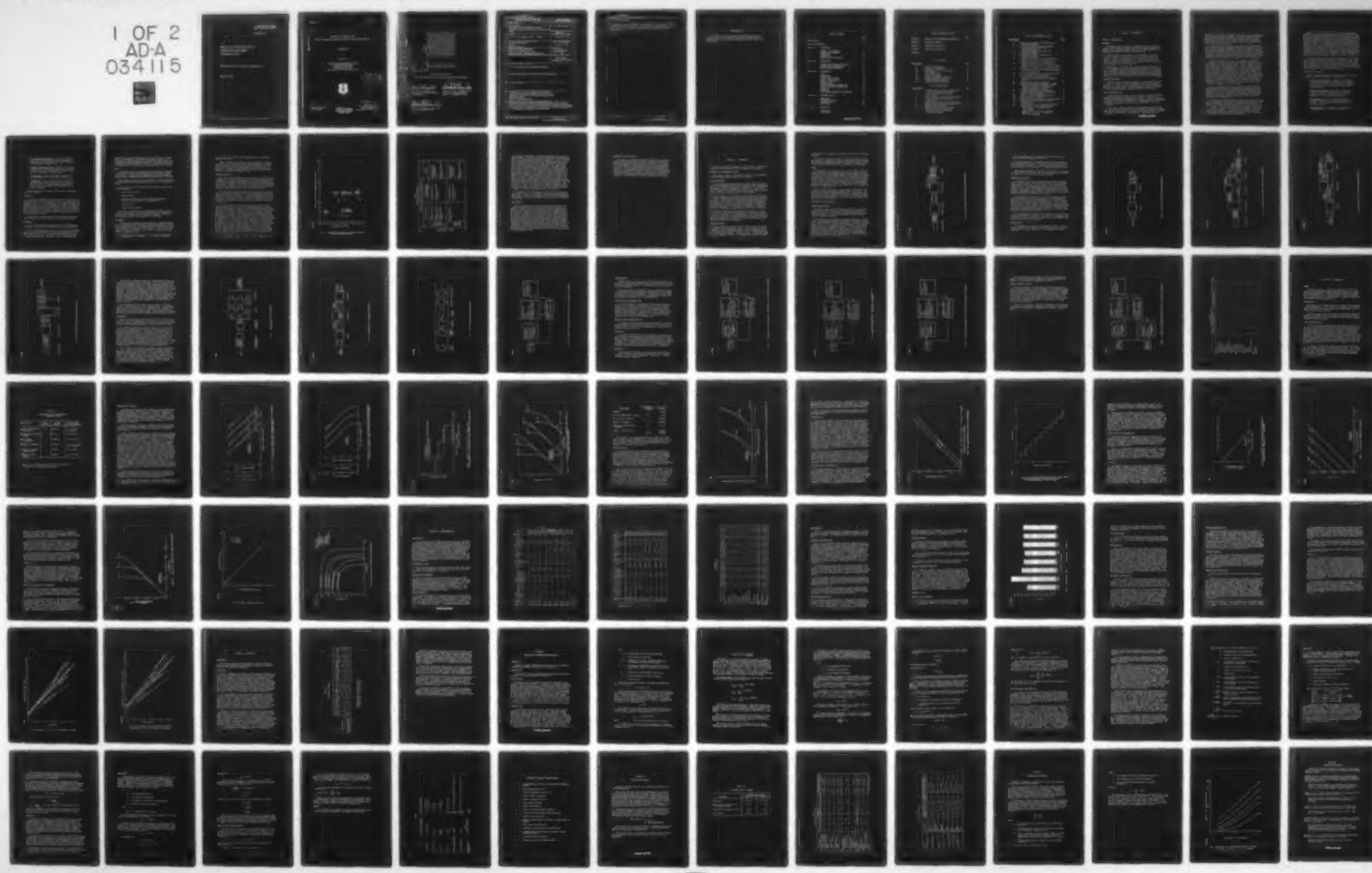

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MODULAR C(3) ARCHITECTURE DIGITAL COMMUNICATIONS INTERCONNECT ALTERNATIVES STUDY

MITRE CORPORATION, BEDFORD, MASSACHUSETTS

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MODULAR C^3 ARCHITECTURE
DIGITAL COMMUNICATIONS INTERCONNECT ALTERNATIVES STUDY

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This report presents the results of examining and analyzing different design approaches of interconnect systems that would handle the transfer of digital information among consoles, computers, mass storage devices, and similar equipments of future modular tactical command and control centers.

20. ABSTRACT (Concluded)

Eight interconnect system alternatives were analyzed and were compared on the basis of performance, cost, and reliability. The alternatives included variation of communications circuit switching, message switching, and bus communications interconnections.

ACKNOWLEDGMENT

This report has been prepared by The MITRE Corporation under Project No. 6030. The contract is sponsored by the Electronic Systems Division, Air Force Systems Command, Hanscom Air Force Base, Massachusetts.

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SECTION I. INTRODUCTION

CONTEXT OF THE ANALYSIS

Objective

The Modular Command, Control, and Communications (C^3) Analysis project has the purpose of establishing a set of common hardware and software modules from which future Tactical Operating Centers can be assembled with maximum flexibility, at minimum cost.

Previous analysis work conducted for the Modular C^3 project justified the use of a wideband, coaxial cable-based communications network to support an integrated audio, video, and data system for information transfer among modules. The analysis reported in this document examines the alternative means by which digital data service can be provided in the wideband network.

The digital data subsystem must provide adequate performance in terms of throughput capacity, access time, and connectivity, and must do so at reasonable cost and with reasonable reliability. A proper choice of digital interconnect architecture requires an understanding of the alternatives available and their comparative capabilities and limitations. The study was conducted to provide such an understanding.

Requirements Assumed

The interconnect requirements assumed for the Modular C^3 analysis are typical of a large, tactical operating center. They include an interface to external digital communications, computers, mass storage devices, and a large number of display terminals. Specific numbers for data rates and response times are presented in Section III.

Scope of the Analysis

The analysis addresses the overall question of center-wide digital communications between a computer system, consoles, a mass storage system, and an external communications interface. Alternative approaches to supporting the necessary information exchange among these modules were evaluated on the basis of three criteria: performance, cost, and reliability.

These three criteria, while of prime importance, cannot form the entire basis for a decision on the most appropriate interconnect approach. Other factors, some of which are more qualitative, must also be carefully considered. These include: deployability, transportability, and

flexibility with respect to changes in operating center configurations, and anticipated growth requirements. The criteria evaluated during the analysis reported in this document serve to eliminate certain interconnect alternatives from further consideration and thereby permit future work to be concentrated on those few candidates which survived this initial screening.

To further clarify the scope of the analysis, three important factors which can affect interpretation of the results must be mentioned here. First, the message statistics assumed are oriented towards a centralized processing architecture, typical of the current generation of tactical operating centers. However, as Section III of this report demonstrates, the final conclusions are largely insensitive to message statistics, so substitution of smart consoles or other types of distributed processing would not, by itself, alter the conclusions.

Second, the question of static versus dynamic connectivity - i.e., whether the connectivity pattern is fixed during system operation, or changed on a rapid and dynamic basis - is not answered in this study. The choice depends primarily upon the processing architecture which is adopted in the operating center. These processing options have a wide range. At one extreme is a static star connection from consoles and external interfaces to a central computer system. At the other extreme is a system where smart consoles and other devices access a number of different processors, memories, and storage devices under program control, using the interconnect to implement such access. However, even though the necessary study to determine a preferred approach has not yet been conducted and the question is left open throughout the analysis, the impact of its answer on interconnect selection is presented in the conclusions.

Third, the analysis is limited to center-wide information exchange among principal elements (modules) of the system. It does not consider the second level of interconnection within these basic system elements, nor does it address explicitly the possibility that components of these system elements (for instance, CPUs or memory modules in the computer system) might be individually attached to this center-wide interconnect.

Conventional engineering practice would indicate that this second level, intracomputer or intraconsole interconnect be built as a high-speed (40 to 80 Mbps) word-parallel, baseband bus, like the DEC Unibus or Intel 8080 address and data buses. Within a limited area, i.e., a few feet, such an approach permits modularity in memory size and CPU power. Because a bus of this sort can operate at CPU cycle speed, implementation of a sophisticated multiprocessor operating system is practical, including such features as fail-soft reallocation of functions to processors, and load balancing.

However, the option does exist of placing these lower level modules (e.g., CPUs and memories) directly on the center-wide interconnect. This provides added flexibility in the physical placement of devices throughout the center, but at the expense of slowing system operation and complicating the operating system which must, as a consequence, handle the resulting delays and resolve competition for computing resources. The delays result because word-parallel buses operating at CPU cycle speeds are not easily extendable for the many hundreds of feet needed in large operating centers. In addition, the presence of electromagnetic noise due to radars and power cabling, fluctuating ground voltages, and other environmental problems require a combination of superior error performance and operating speed which might well prove prohibitively expensive. In this environment, a slower interconnect, running at a speed like 10 Mbps is more practical.

The trade-off between a high-speed/low-speed, local area/center-wide, hierarchical interconnection and a single-level, lower speed interconnection was beyond the scope of this study. However, the ability to support the necessary information exchange in a single level interconnect is dependent upon the ability to dynamically alter connectivity patterns. As mentioned earlier, the impact of providing that capability is identified in the conclusions.

ALTERNATIVES CONSIDERED

Eight alternative approaches to the design of an interconnect system were identified as worthy of consideration.

- A Static Circuit Switch - consisting of a computer-controlled patchboard using modern digital technology to provide a fixed set of connections among subscribers which are usually altered only during system reconfiguration;

- A Dynamic Circuit Switch - similar to the static circuit switch with the exception that only those circuits currently in use are kept connected, analogous to conventional voice telephone;

- A Message Switch - in which subscribers transmit packets of data, bearing destination addresses, to a central computer which then routes them to the intended recipient;

- A Contention Bus - in which all subscribers share a common channel and contend for access to it;

- A Static Dedicated Slot Bus - in which all subscribers share a common channel and each transmits in designated time slots which are usually altered only during system reconfiguration;

- A Dynamic Dedicated Slot Bus - similar to the static dedicated slot bus with the exception that slots are assigned only to those subscribers currently active, and are reassigned on a dynamic basis;

- A Polled Bus - in which subscribers transmit only when interrogated by the bus control element; and

- A Loaned Bus - which is like a polled bus with the exception that polling, signalling, and supervision are carried on a separate frequency channel from data to achieve more efficient utilization of data channel capacity.

These alternative interconnect architectures are defined in detail in Section II.

CONCLUSIONS

The primary conclusion of this study is that three of the alternatives considered - the static circuit switch, the dedicated slot assignment bus, and the contention bus - are clearly preferred to the others with respect to cost and reliability. There is no particular distinction among any of the alternatives in terms of performance within the context of this study. Within this preferred group, the choice is influenced by the relative importance of cost, reliability, growth capability, and the need to rapidly reconfigure connectivity patterns within the system.

Each of the three basic criteria is discussed in more detail below, followed by an examination of their interrelationships.

Performance

All of the alternatives analyzed meet the stated performance requirements with respect to throughput capacity and access time.

It is worth noting, however, that the bus designs are inherently more powerful than the message and circuit switching designs in the sense that they can support more throughput with shorter response time at lower cost than can the others. This distinction becomes significant when required throughput capacity grows substantially

beyond the anticipated requirements of Modular C^3 Centers. In addition, the bus designs can also support more rapid alteration of connectivity patterns within the center than can the other approaches. The ability to sustain substantial growth at relatively low cost and to dynamically alter connectivity are important collateral features.

Cost

Procurement costs for the different alternatives were estimated, in terms of both non-recurring (development) and recurring (production) elements. Operating and maintenance costs were not estimated because detailed information on operating scenarios was not available.

Non-recurring costs are about the same for all of the alternatives except the dynamic circuit switch which proved to be 30 percent more costly.

Recurring costs for the different systems rank as follows, from lowest to highest:

- Static Circuit Switch;
- Message Switch;
- Contention, Static Dedicated Slot, Dynamic Dedicated Slot, and Polled Buses, all of comparable cost;
- Loaned Bus; and
- Dynamic Circuit Switch.

The cost of each alternative increases as the number of subscribers increases, but if ten or more subscribers are involved, the ranking does not change nor does the ranking change if the total of non-recurring costs plus recurring costs is considered.

Reliability

Reliability was considered in two categories: single-subscriber service reliability (that is, the mean-time between failure of service for a single subscriber), and system reliability (mean-time to failure of any component of the system). The former is of most concern with regard to operational impact, and the latter is of most concern with respect to maintenance costs.

The alternatives considered fall into two distinct groupings for single-subscriber service reliability. In the more reliable group

are the static circuit switch, the contention bus, and the static dedicated slot bus.

Control computers are the least reliable elements of those systems where their use on a real-time basis is essential. Therefore, these systems are inherently less reliable than those which do not require them. This factor distinguishes the first group from the remainder. Redundant computers can be employed to increase system reliability, but only at additional cost.

Interrelationships

The results of considering cost and reliability jointly are shown in Figure 1. The relative performance of the different approaches is illustrated with respect to production cost for a 100-subscriber system and single subscriber failure rate (the inverse of single subscriber reliability). The axes on the chart are so defined that the interconnect alternative closest to the origin is the most desirable, since it possesses a combination of low cost and low failure rate.

Three approaches stand out: the static circuit switch, the static dedicated slot bus and contention bus for low failure rates, and the static circuit switch for low cost. All other alternatives are further from the origin than these three. The relative weighting of cost and reliability can determine the choice between the static switch and the two buses. No weighting will make the others preferable to some one of these three.

Cost and reliability can be traded for one another in these designs by duplication of the least reliable elements of the system. This trade-off is shown in Figure 1 by the dotted arrow associated with each of the alternatives. For the static circuit switch, the subscriber interface units and the switching matrix are of roughly comparable reliability. Provision of two separate switching matrices with automatic switchover would cost about $60,000 for a 100-subscriber system, and would decrease failure rate by about 17 percent. A similar increase in reliability can be achieved with the simple buses by duplicating the bus repeater, at a cost of about $1,500. This brings the buses and the static circuit switch close together on the plot. For the remaining alternatives, the least reliable element is the control computer; its duplication will nearly double reliability, but at a cost of about $10,000. However, even though the reliability of these alternatives can be further improved so that the lower failure rate of the simpler buses is achieved, this can be accomplished only at a substantially greater total cost.

The factors which influence a choice among the three best alternatives are illustrated further in Table I. Three columns are shown

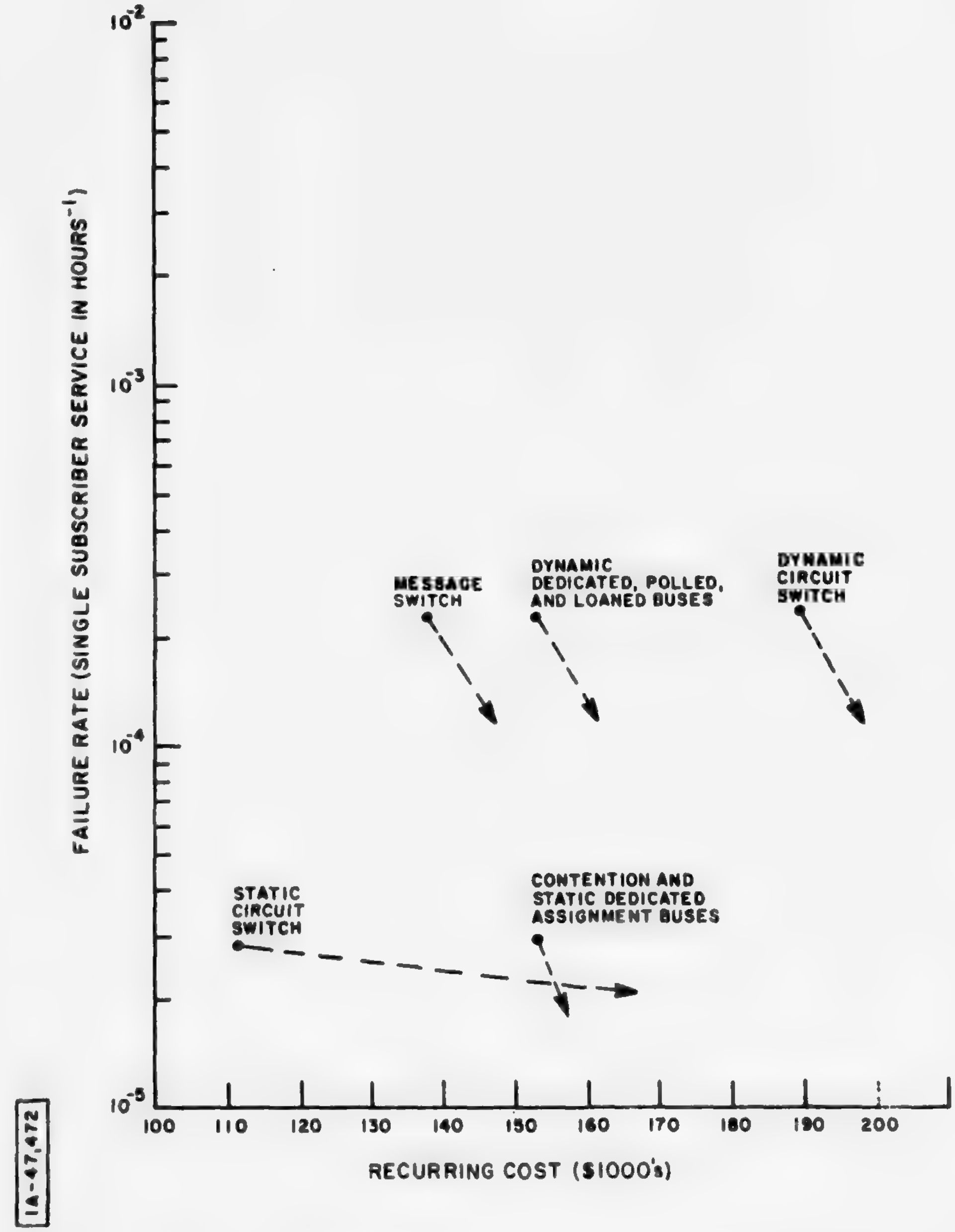

Figure 1. FAILURE RATE AS A FUNCTION OF RECURRING COST FOR 100-SUBSCRIBER SYSTEM

TABLE I

PREFERRED ALTERNATIVES

COST VS. RELIABILITY	DYNAMIC CONNECTIVITY-CHANGE CAPABILITY: NEVER REQUIRED	MAY BE NECESSARY IN THE FUTURE	REQUIRED
RELIABILITY MORE IMPORTANT	● CONTENTION BUS; or ● STATIC DEDICATED SLOT BUS; or ● STATIC CIRCUIT SWITCH	● CONTENTION BUS; or ● STATIC DEDICATED SLOT BUS	● CONTENTION BUS WITH UPGRADED CONTROLLER; or ● DYNAMIC DEDICATED SLOT BUS
COST MORE IMPORTANT	● STATIC CIRCUIT SWITCH	● CONTENTION BUS; or ● STATIC DEDICATED SLOT BUS	● CONTENTION BUS WITH UPGRADED CONTROLLER; or ● DYNAMIC DEDICATED SLOT BUS

in this table. Each denotes a different possibility with respect to the requirement to dynamically change connectivity patterns among the users in the center while the system is operating. If such a requirement is never expected to pertain (for example, because the center-wide interconnect is part of a two-level, hierarchial interconnect scheme like that discussed earlier) then either the simple buses or the static circuit switch are satisfactory. The final choice depends upon the relative importance of cost and reliability to the user. If low cost is of prime importance, then the circuit switch is preferable because it can be made more cheaply than the buses. However, when reliability of one service failure per subscriber per 20,000 hours or better is desired, the buses become cheaper. If a dynamic connectivity change capability is, or may be required (for example, in order to implement the entire interconnect system on a single hierarchial level supporting extensive distributed processing) the static circuit switch ceases to be a serious contender. The reason is that the penalty in both cost and reliability associated with upgrading the static circuit switch to provide the dynamic capability is severe; it becomes the dynamic circuit switch shown in Figure 1. The penalty involved in upgrading the buses is much less.

In summary, joint consideration of these factors indicates that either a switch or a bus is satisfactory for currently hypothesized requirements. However, if a dynamic connectivity-change requirement is anticipated, buses are preferable from both a cost and reliability point of view.

FURTHER WORK

The work reported in this paper represents the initial steps in the selection and design of a digital interconnect subsystem for Modular C^3 systems. As was noted earlier, the conclusions are conditional upon the need for a dynamic connectivity change capability which, in turn, depends upon the processing architecture adopted. The question of whether or not such a need exists should be resolved by a study, similar in scope and level of detail to this one, but addressed to the definition of processing modules (including memory, central processing units, and operating system software) for both consoles and any central computer system. The resulting definition of processing modules and their communications requirements should be considered in conjunction with both a definition of video and voice requirements and the results of the study reported here. This will permit the design of a cost-effective solution to the total processing and communications problem.

ORGANIZATION OF THE REPORT

This paper is organized as follows: Section II presents a more detailed description of the alternatives analyzed in this study, Section III presents the details of the analysis of these alternatives with respect to their performance, Section IV discusses the cost of the different alternatives, and Section V discusses their reliability. Four Appendices follow which present detailed derivations of the performance results in Section III, reliability data supporting Section V, a discussion of time slot queuing pertaining to the slot assignment buses, and a bibliography of literature relevant to the performance of message switching and bus systems.

SECTION II. ALTERNATIVES

This section provides descriptions of the specific communications interconnect architectures which were analyzed in this study.

COMMUNICATION INTERCONNECT CLASSES

Three generic classes of interconnect approach were considered: circuit switching, message switching, and busing.

Circuit Switching

Circuit switching systems are those in which individual connections are established among devices or users who wish to communicate. Each user is provided a unique circuit connection to a central switching device which has the capability to connect any circuit to any other. Provisions are made at the central unit to process connection requests and react to busy conditions in the network.

For the purposes of this analysis, two principal variations of the circuit switching approach were considered. The first variation is a static circuit switch. This approach provides semi-permanent connections. These connections remain intact while the system is in its normal mode of operation. Connectivity changes are made only when the system is being reconfigured, augmented by the addition of new mission equipment, or experiencing an emergency. In essence, this form of circuit switching is simply an electronic patchboard.

The second variation is the dynamic circuit switch. In this approach, user or device interfaces initiate connectivity requests to a switch controller for all transmissions. The controller establishes and maintains all interconnections for the period required to complete the information transfer, and then releases them. This is closely analogous to voice telephony.

Message Switching

Message switching systems are those in which users or devices communicate via an intermediary device. The intermediary, normally a computer, accepts information from all devices, temporarily stores the information and subsequently forwards it on a message-by-message basis to intended recipients. Discrete messages, or packets comprising segments of messages, include the necessary information to indicate

the originator or identity of the information as well as the intended recipient.

A variety of storage and control structures for support of message switching are possible. However, since all share the same basic characteristics, differing only in details, only one generic version of the message switching approach was included in this analysis.

Busing

Bus communications systems are those in which users or devices communicate over a common channel and employ the technique of continually addressing each communication. In bus systems, many messages can coexist, but all carry unique addresses which permits any one to be distinguished from all others. A typical system is time-shared, allowing users to transmit information in short duration, high-speed bursts. In most bus designs, all transmissions are synchronized to a common timing source. Information bursts from users are either permitted to contend for access to the channel or not, depending upon the specific implementation.

The five principal variants of bus systems - contention, static assignment, dynamic dedicated assignment, polled and loaned - are among the alternatives analyzed in this study. Distinctions among the variants are associated with the manner in which the transmission capacity of the common channel is allocated and the method by which channel access is controlled.

COMMUNICATION CONFIGURATIONS

Static Circuit Switch

The static circuit switch alternative consists of a controller and subscriber interface units. The controller consists of an operator console, a control computer, a switch matrix, and modems, as shown in Figure 2. Each modem connects by a point-to-point link to a specific subscriber.

The operator console consists of a keyboard and display device. It permits the following actions by the operator: (a) input of connectivity change commands to computer and display, (b) monitor and display system status, and (c) technical control processing. The control computer performs the following functions: (a) processing of con-connectivity change commands and output thereof to the switch, (b) monitoring of system status and transferring it to the console on demand, (c) collecting of usage satistics and transferring them to the console on demand, and (d) performing fault isolation processing either automatically or under console control.

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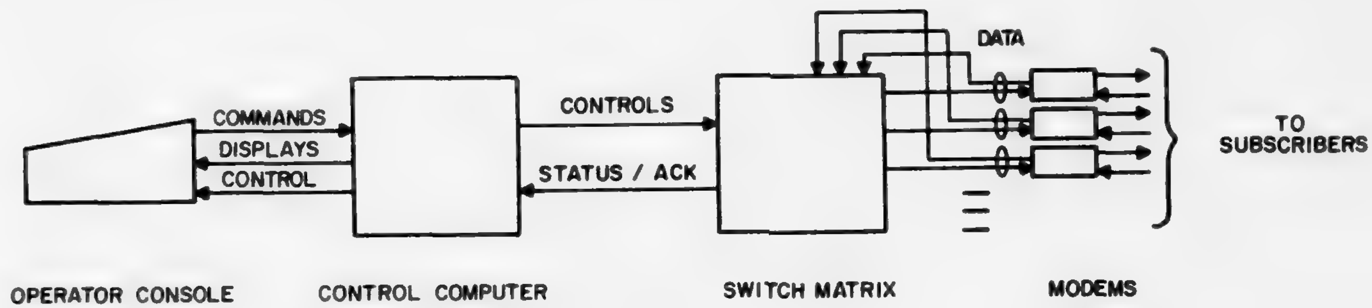

Figure 2 STATIC CIRCUIT SWITCH CONTROLLER CONFIGURATION

The size and speed of the computer is determined by the rate at which connectivity changes must be made.

The switching matrix is constructed of large scale integrated (LSI) digital switch components, such as those built by Sperry Univac and described in Reference 1. The switch connects/disconnects circuits as commanded, reports status, and supports diagnostic software.

The subscriber interface unit (SIU), shown in Figure 3, consists of a modem and interface logic. The logic performs serial-to-parallel conversion as well as level and timing conversion.

<u>Dynamic Circuit Switch</u>

The dynamic circuit switch consists of the elements discussed above, but with a faster, more powerful computer, and a multiplexer connecting all subscribers to the computer. This configuration is shown in Figure 4. The multiplexer intercepts connectivity change requests from individual subscribers and transfers them to the control computer. The computer then commands the switching matrix to establish the appropriate connections and/or sends a reply to the requesting subscriber indicating the status of his request.

The multiplexer functions as a call register handling command/status exchanges with the control computer. It accepts address requests from the terminals, transfers them to the control computer, and monitors the control computer response times. If the response indicates that the line is busy, the multiplexer informs the terminal. If the response is an acceptance, the multiplexer informs the terminal and monitors the terminal status to determine call termination time. At that time, the multiplexer issues a message to the control computer informing it that the call has ended.

The configuration of the subscriber interface unit for the dynamic circuit switch is shown in Figure 5. In addition to performing all of the functions of the static circuit switch SIU, the multiplexer logic section must also perform buffering.

<u>Message Switch</u>

The message switch consists of an operator console, control computer, multiplexer, and modems. Each modem connects via a point-to-point link to a specific subscriber. The configuration is shown in Figure 6.

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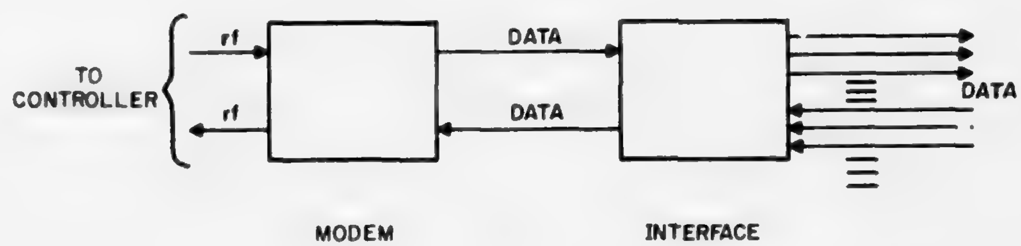

Figure 3 STATIC CIRCUIT SWITCH SUBSCRIBER INTERFACE

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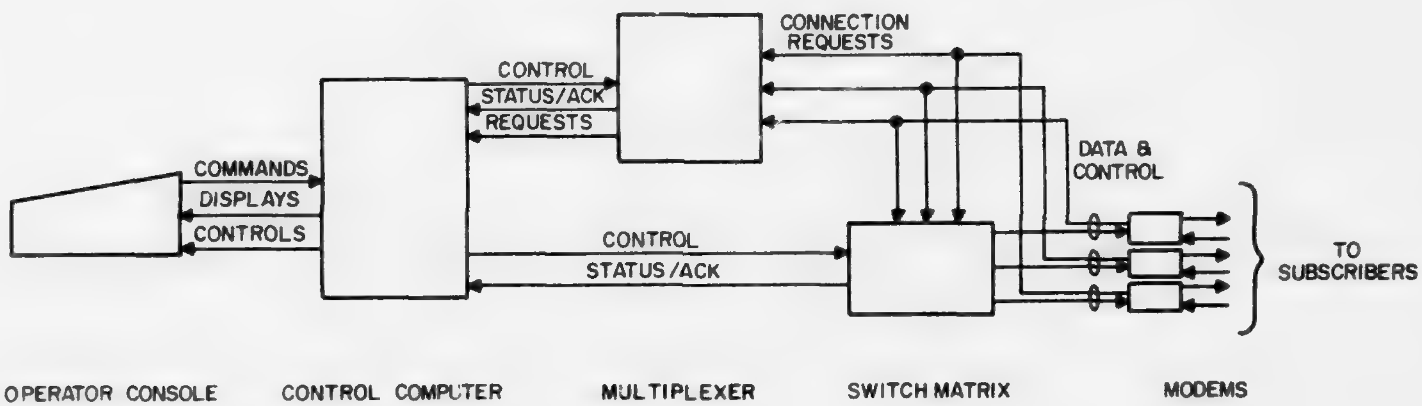

Figure 4 DYNAMIC CIRCUIT SWITCH CONTROLLER CONFIGURATION

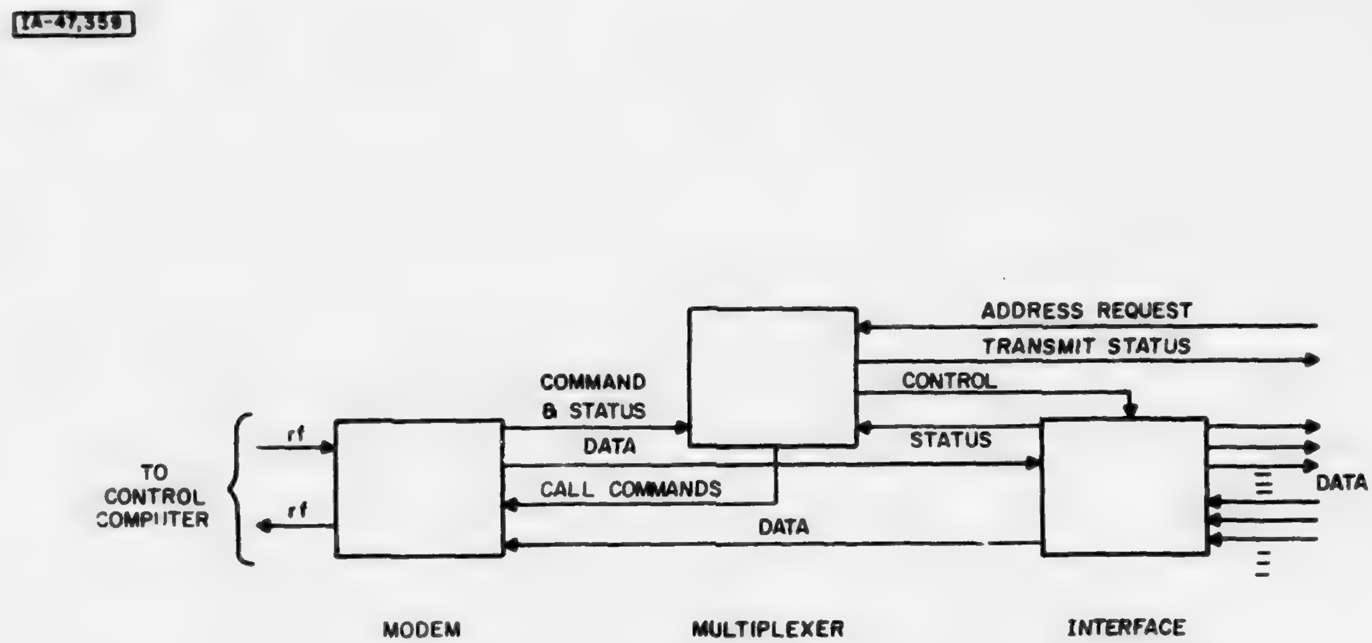

Figure 5 DYNAMIC CIRCUIT SWITCH SUBSCRIBER INTERFACE

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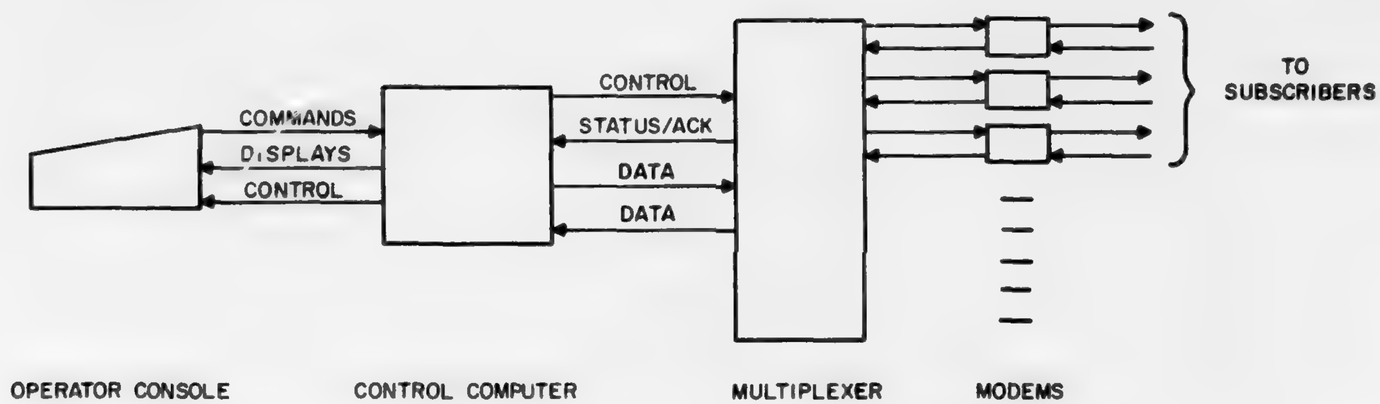

Figure 6 MESSAGE SWITCH CONTROLLER CONFIGURATION

The console is used by an operator to monitor system status, and to assist in technical control processing. The control computer performs the following functions: (a) routes incoming messages to the appropriate addressee, (b) monitors system status and transfers status data to the console on demand, (c) collects usage statistics and transfers them to the console on demand, and (d) performs periodic self-test functions. The multiplexer performs the following functions: (a) maintains interfaces to all subscribers, (b) buffers and transfers data between all subscribers and the control computer, and (c) reports status. Unlike the dynamic circuit switch multiplexer, which intercepts and transfers request messages only, the message switch multiplexer transfers all data received from and transmitted to all subscribers, as shown in Figure 7.

The configuration of the SIU is shown in Figure 8. This SIU consists of a modem, controller, and interface logic. The modem and interface logic are similar to their counterparts in a dynamic circuit switch system, but the controller is less complex since destination addresses are included in message headers. The controller also monitors and reports status, and reacts to commands from the network controller.

Bus Systems

The hardware configuration is similar for each of the bus system variations. The bus configurations all consist of an operator console, a control computer, a bus repeater, and bus interface units interfaced directly to the individual subscribers. This is shown in Figure 9.

The functions performed by the bus console are similar to those performed by the message switch console. The control computer performs the following functions: (a) processing connectivity control, (b) monitoring system status and transferring it to the console on demand, (c) collecting usage statistics and transferring them to the console on demand, (d) performing periodic self-test functions, and (e) performing fault isolation processing either automatically or under console control. The data bus repeater repeats onto the outbound bus all data received from interface units on the inbound bus. It also performs: (a) modulation/demodulation, (b) idle sequence generation between messages, and (c) synchronization message generation.

Most of the bus SIU elements are common to all bus alternatives, i.e.: (a) a modem is required to modulate and demodulate signals, (b) high-speed receive logic is required to detect system and message synchronization, maintain a bit count, and maintain timing for transmission, (c) low-speed receive logic is required to perform parity checks, filter received messages, and process commands, (d) I/O logic is required to handle user protocols, and (e) low-speed transmit logic is required to form status messages and format transmit messages. Figure 10 shows these basic functional elements.

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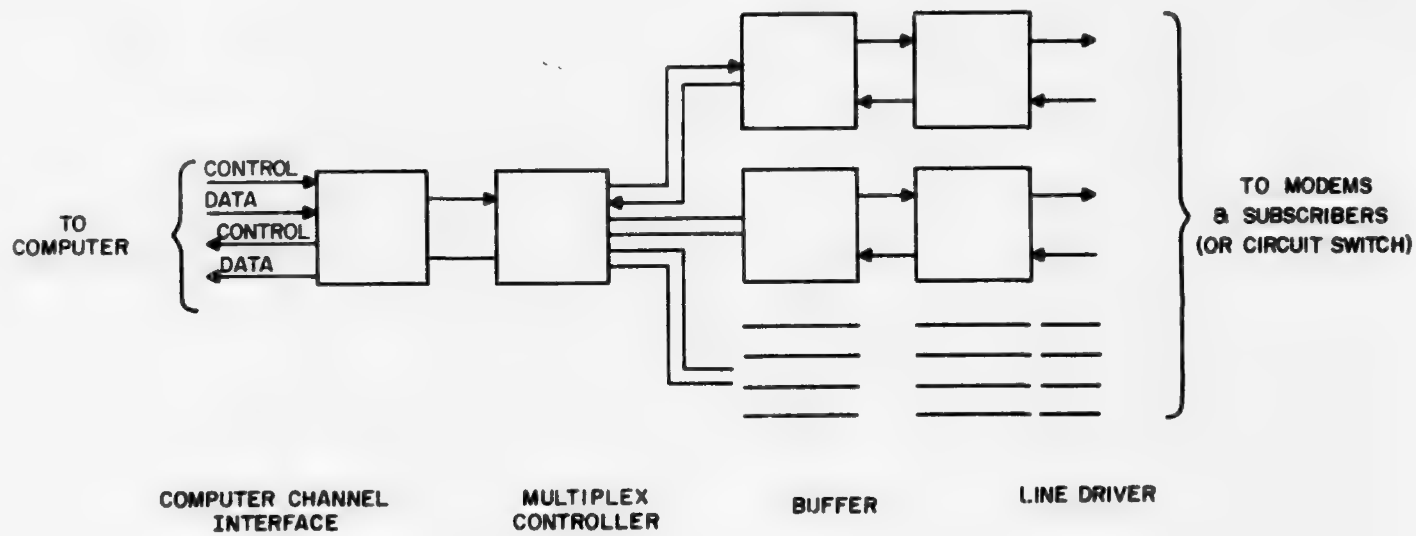

Figure 7 MESSAGE SWITCH - MULTIPLEXER

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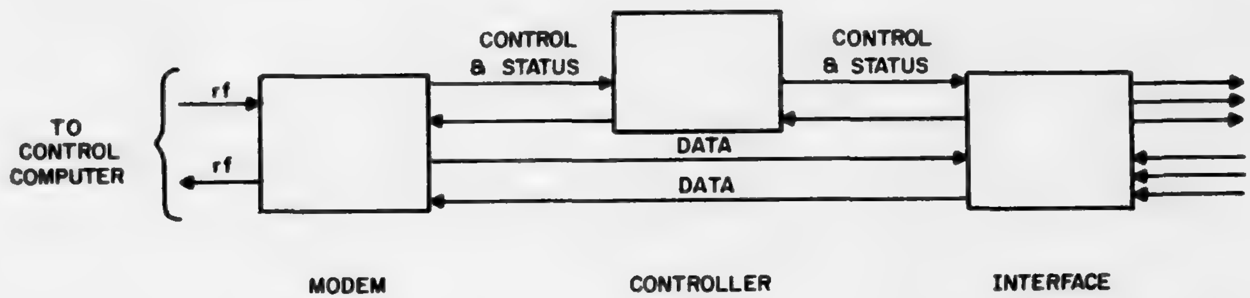

Figure 8 MESSAGE SWITCH SUBSCRIBER INTERFACE

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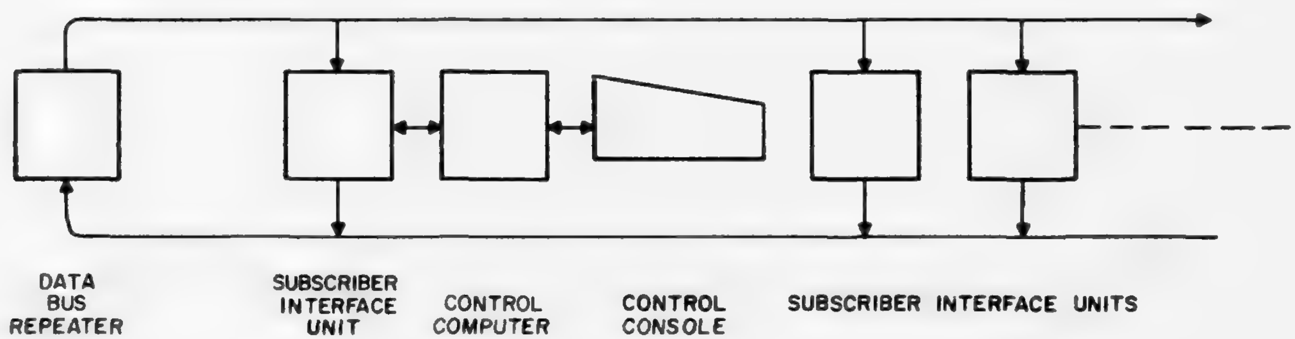

Figure 9 BUS SYSTEM–GENERAL CONFIGURATION

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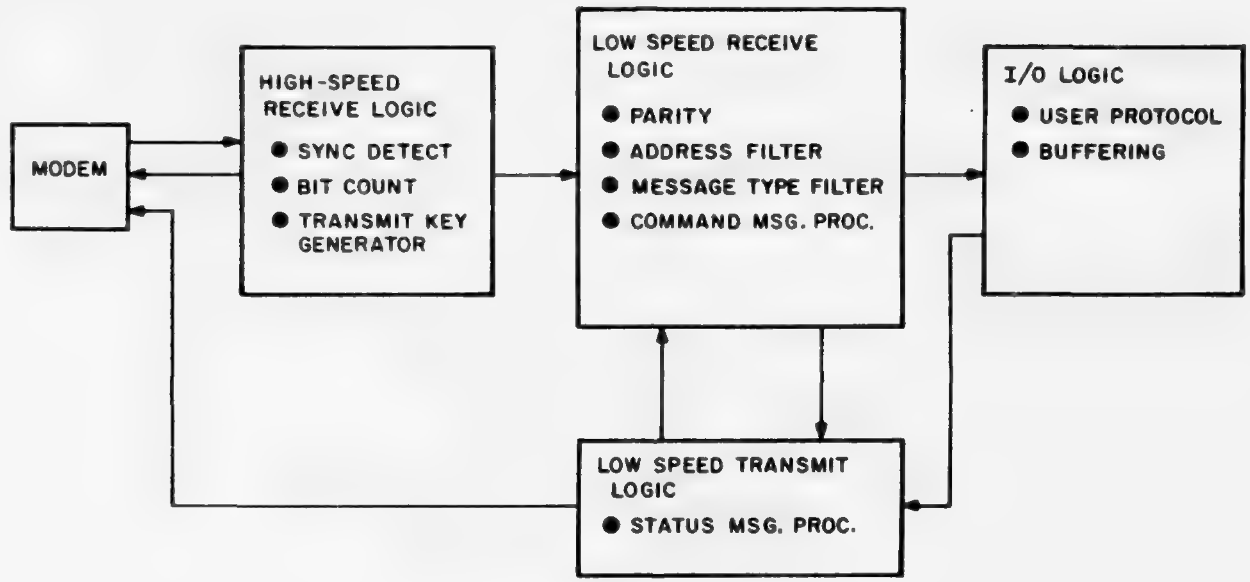

Figure 10 COMMON SUBSCRIBER INTERFACE UNIT FUNCTIONAL ELEMENTS

Contention Bus

Figure 11 shows the functions of the contention bus SIU. The functions, unique to the contention alternative, are a valid transmit check and a retransmit control. The remainder are common among all the bus alternatives.

The valid transmit check monitors the bus to determine whether or not a message has been successfully transmitted. If the message is blocked, it must be retransmitted. The retransmit control logic is responsible for retransmitting the message after a random delay. This reduces the probability of a second blocking.

Static Dedicated Assignment Bus

The static dedicated assignment bus SIU is shown functionally in Figure 12. In addition to the common functions, this alternative requires slot synchronization and slot count in the low-speed receive logic to permit the SIU to use its assigned slots and not interfere with another unit's communication. This alternative also requires a request message processor. The logic generates requests for system access and for address change. The time slot keying function ensures bit and slot synchronization.

Dynamic Dedicated Assignment Bus

The dynamic dedicated assignment bus SIU has all of the functions contained in the static dedicated assignment bus SIU. However, its request message processor is more complex since it permits the SIU to request changes in data rate.

Polled Bus

The unique functions which are incorporated in a polled bus SIU are the message synchronization and the automatic response. This is shown in Figure 13. The message synchronization logic is in lieu of the slot and frame synchronization logic associated with the dedicated assignment bus. If there is no message for transmission when the SIU is polled, the automatic response logic transmits a status report to inform the network control element that the unit is operational.

Loaned Bus

The loaned bus SIU requires a separate modem and high-speed control logic to handle control message transfers. This is the only alternative that has control information transmitted on a frequency different from data information.

IA-47,364

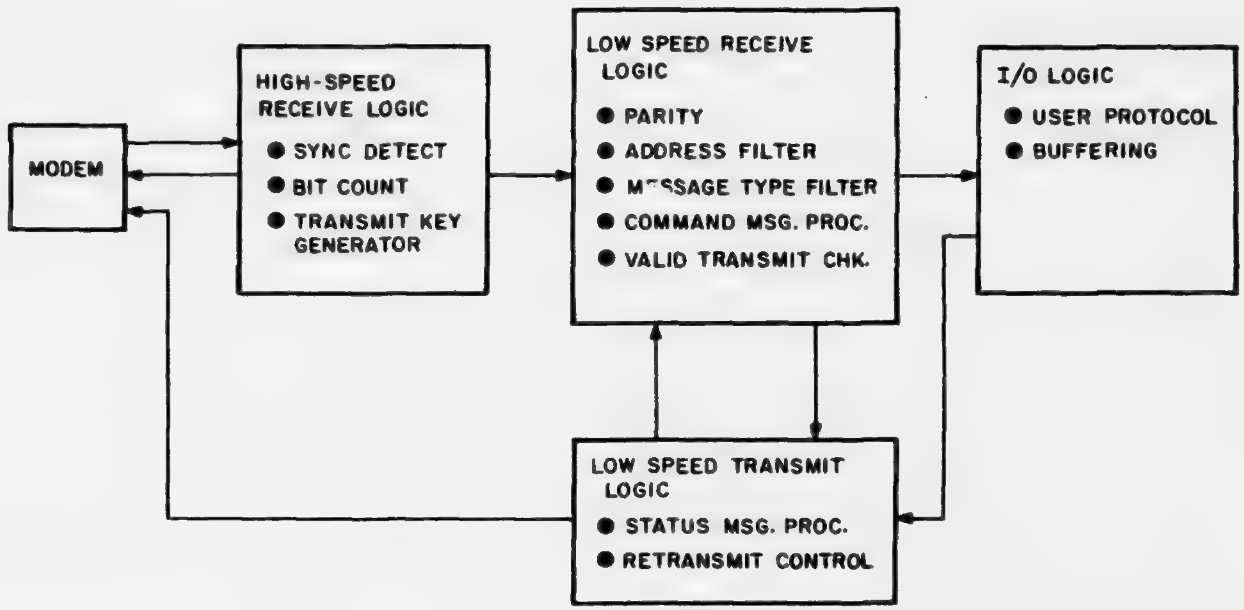

Figure 11 CONTENTION BUS SUBSCRIBER INTERFACE UNIT FUNCTIONAL ELEMENTS

IA-47,360

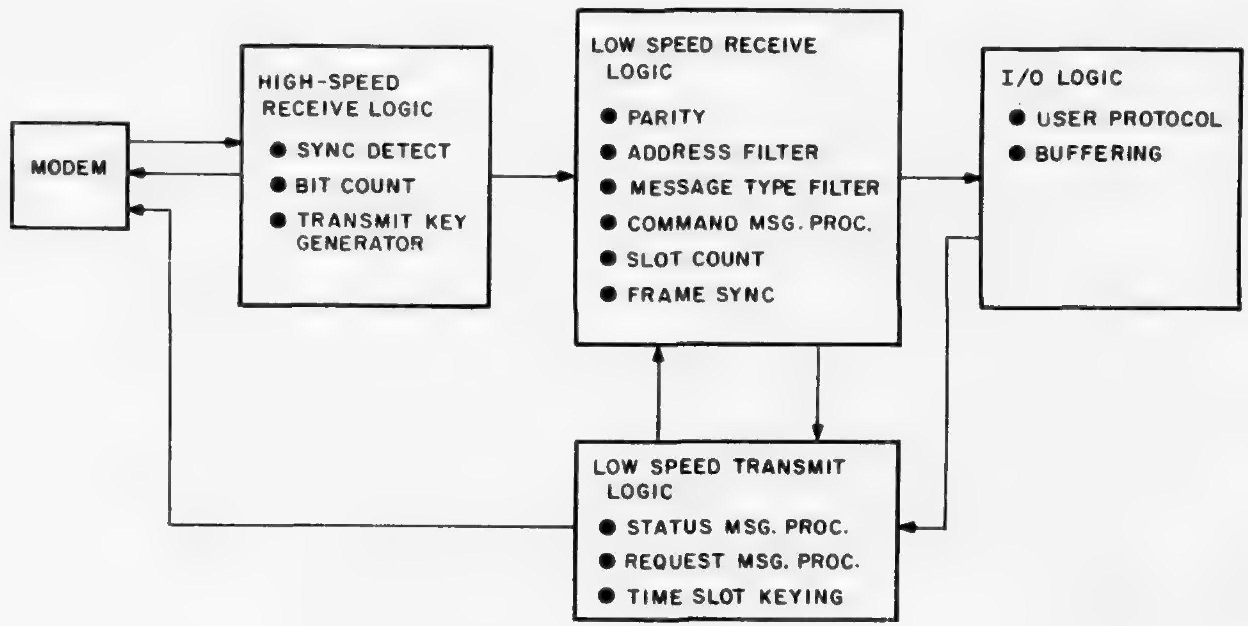

Figure 12 STATIC AND DYNAMIC DEDICATED ASSIGNMENT BUS SUBSCRIBER INTERFACE UNIT FUNCTIONAL ELEMENTS

IA-47,361

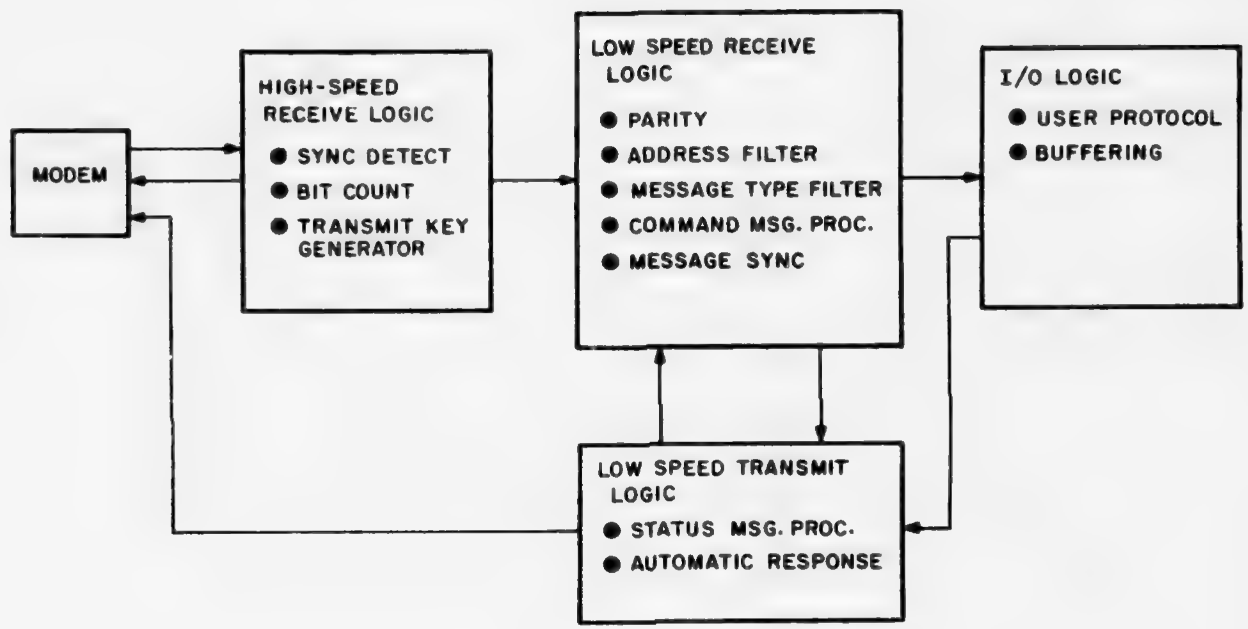

Figure 13 POLLED BUS SUBSCRIBER INTERFACE UNIT FUNCTIONAL ELEMENTS

The loaned bus SIU also requires a unique request message processor. This logic constructs requests for the entire system data bandwidth. The functions are summarized in Figure 14.

CONTROL COMPUTER SOFTWARE

The control computer performs slightly different functions for each of the alternatives, as outlined earlier. In all cases, standard executive functions, including: task scheduling, interrupt handling, error recovery, and initial loading routines are required. Although they differ in detail, system initialization functions are required in all cases since connectivity patterns must be established and entries made in system status tables. In all cases, console routines are required to support interaction with an operator for command entry and report generation.

Routines are required to support the differing control functions of the various alternatives, as summarized in Table II. Amplifying information on program size is estimated and presented in Section IV, Cost.

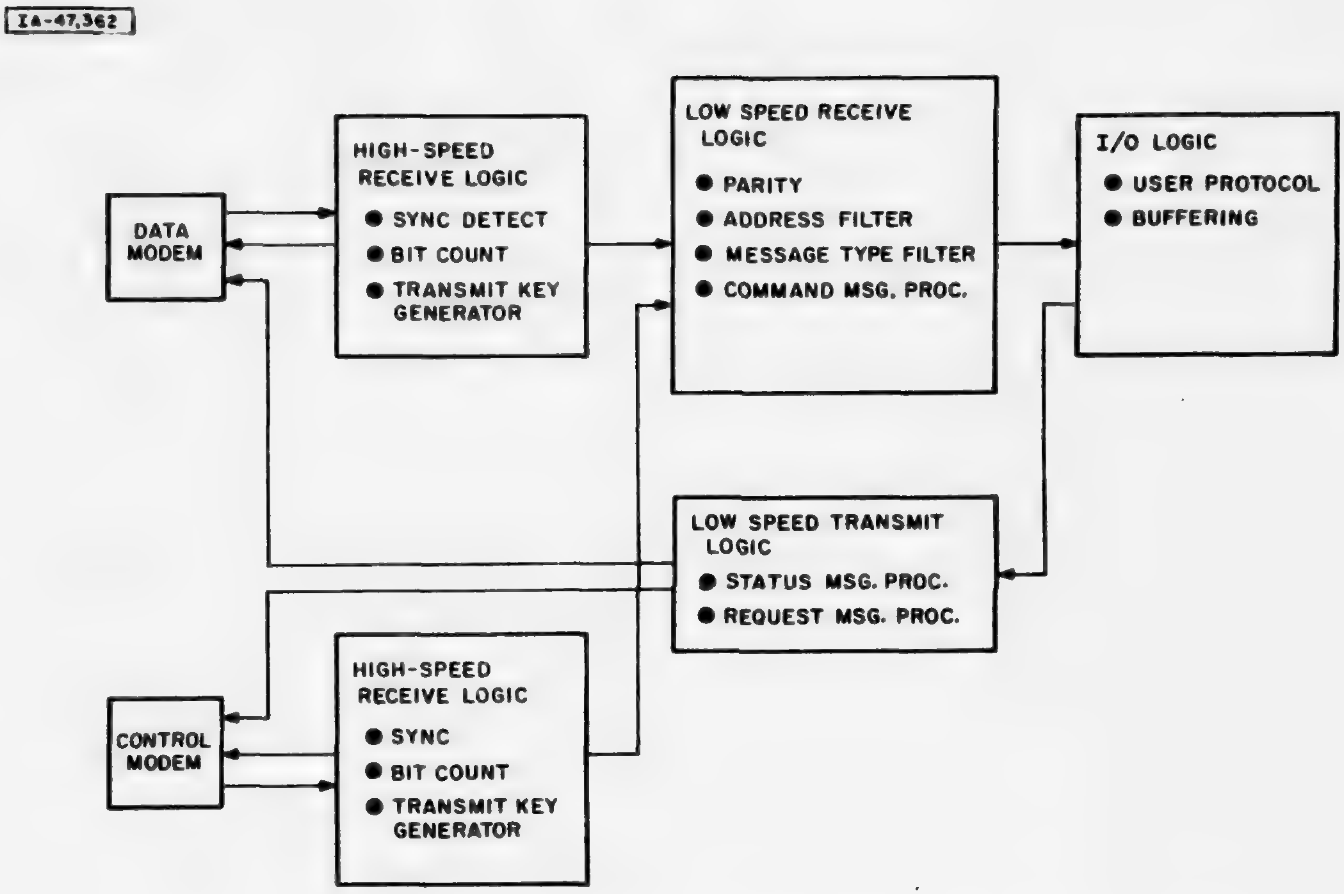

Figure 14 LOANED BUS SUBSCRIBER INTERFACE UNIT FUNCTIONAL ELEMENTS

TABLE II

SOFTWARE CONFIGURATIONS

	STATIC CKT SWITCH	DYNAMIC CKT SWITCH	MESSAGE SWITCH	CONTENTION	STATIC DED. ASSIGNMENT	DYN. DED. ASSIGNMENT	POLLED	LOANED
EXECUTIVE								
TASK SCHEDULING	X	X	X	X	X	X	X	X
INTERRUPT HANDLING	X	X	X	X	X	X	X	X
ERROR RECOVERY	X	X	X	X	X	X	X	X
INITIAL LOAD	X	X	X	X	X	X	X	X
INITIALIZATION								
TABLE MAINTENANCE	X	X	X	X	X	X	X	X
CONFIGURATION SET-UP	X	X			X	X		
CONSOLE ROUTINE								
INTERACTIVE	X	X	X	X	X	X	X	X
REPORT PRINTOUT	X	X	X	X	X	X	X	X
OPERATION CONTROL								
TYPE FILTER		X	X	X	X	X	X	X
STATUS ROUTINE		X	X	X	X	X	X	X
TECH CONTROL		X	X	X	X	X	X	X
REQUEST HANDLER								
ACCESS				X	X	X		X
ADDRESS		X	X	X	X	X	X	X
DATA RATE				X		X	X	X
NETWORK RECONFIGURATION						X		
POLL							X	
DATA FILTER			X					
MESSAGE FORMAT	X	X	X	X	X	X		X

SECTION III. PERFORMANCE

GENERAL

This section discusses performance available from static and dynamic switching systems, message switching systems, and a number of busing system variations. Traffic throughput capacity and access time to successfully enter a message into the interconnect system are discussed for each of the alternatives. Detailed substantiating analyses are presented in Appendix A.

REQUIREMENTS

Requirements for throughput capacity in Modular C^3 Centers have not been established. For the purpose of this analysis, the numbers shown in Table III were assumed; these are a typical worst case for a large tactical operating center.

Access time better than 0.25 seconds to transfer any message is assumed to be adequate. This is a generally accepted standard for the maximum delay which will not interfere with the work of a person using an interactive terminal.

STATIC CIRCUIT SWITCH

The static switching configuration, described in Section II consists of a solid-state switching matrix which provides connectivity paths among system modules. The connectivity paths are established by control-computer and console-entry procedures. This approach, essentially an electronic patchboard, is capable of providing the necessary connectivity paths among several hundred subscribers in any combination. Established connectivity paths are static; that is, they are not changed while the center is in operation. When several separate connections to different modules are required, each connection is implemented through a separate circuit and separate lines to the device.

The number of connectivity paths provided is made sufficient to meet the probable needs of tactical operating centers. The capacity of each link, using hardware of the type cited in Reference 1, is 25 Mbps per line. This capability exceeds the data rate requirements stated in Table III and, since the connections remain established, access time is instantaneous.

TABLE III

HYPOTHESIZED CAPACITY REQUIREMENTS
(MAXIMUM BUSY HOUR)

DEVICE TYPE	DEVICE QUANTITY (K)	MESSAGE LENGTH (b)	AVERAGE MESSAGE RATE TRANSMITTED (α)
INTERACTIVE TERMINALS OR CONSOLES	100	1,000 bits	0.1 per second per terminal
EXTERNAL COMMUNICATIONS (INPUT)*	1	228 bits	30 per second
MASS STORAGE (TO COMPUTER)	1	1 Megabit	0.1 per second
COMPUTER TO TERMINALS	1	10,000 bits	10 = .1 per second x 100 terminals
COMPUTER TO EXTERNAL COMMUNICATIONS*	1	228 bits	30 per second
COMPUTER TO MASS STORAGE	1	1 Megabit	0.1 per second

*Assumes use of JTIDS system for external track reporting at a rate of 30 track messages per second.

DYNAMIC CIRCUIT SWITCH

The dynamic switching approach is similar to that described above for static switching. However, the control computer changes and re-establishes connectivity in real-time as a result of connectivity requests (dialing commands) received at the computer through a call-register which monitors the lines to individual subscribers. A path through the switch is created for each message as it is received from a subscriber and the path is destroyed when transmission of the message has been completed.

The switch capacity required to implement this approach depends upon the following items: message rate distribution, message length distribution, and switch dwell time (time required to establish a given circuit).

Figure 15 shows the quantity (N) of simultaneous circuits through the switching matrix which is required to support the indicated combination of message rate (αK) and message duration. The corresponding message length, in bits, is shown for a circuit bit rate of one Mbps and ten Mbps and the sensitivity of N to switch dwell time (t_d) is shown. These curves are for ten percent probability of exceeding an access time of 0.25 seconds. The quantity (N) required is highly insensitive to access time for the range of access times significant for human operation of a console. This is shown in Figures 16 and 17. Figure 16 plots the quantity of circuits (N) required versus message statistics for a 0.01 second access time; Figure 17 plots the quantity of circuits (N) as a function of probable waiting time in milliseconds for a ten percent probability of exceeding the given access time of .1 and .01 seconds. The total response time is the sum of this waiting time, the time required by a control computer to effect the necessary processing to control the switch, and the switch dwell time. For typical minicomputers and semiconductor switching devices, this total would likely amount to a few tens of milliseconds, at most. The point is that the number of circuits required does not exceed the asymptotic minimum number of circuits at a response time greater than four milliseconds.

Figure 18 replots the quantity of circuits (N) as a function of traffic load (the product of messages per second per subscriber (α) and number of subscribers (K)), and as a function of message length expressed in bits (b), for several switching delays (t_d).

The significance of these curves is indicated by using the values presented in Table III as an example. The following figures are based on information in Table III:

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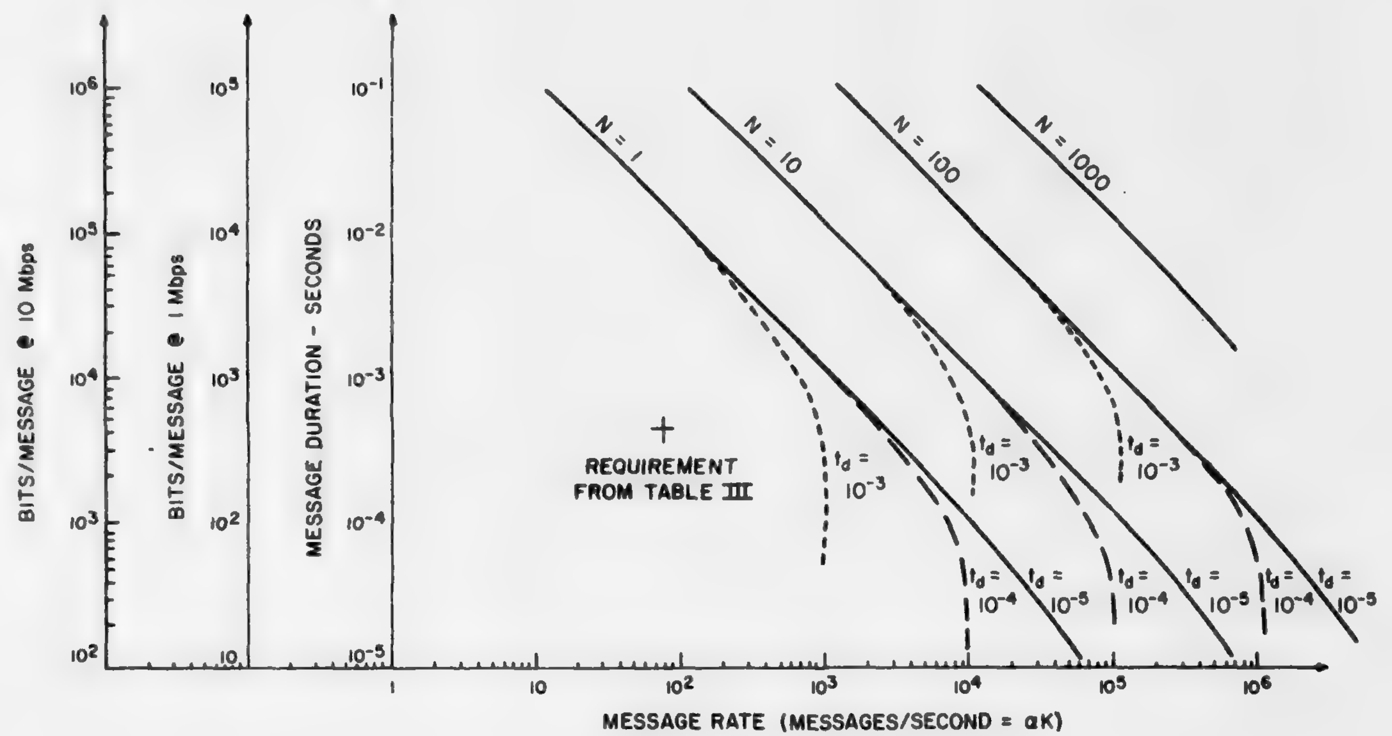

Figure 15 QUANTITY OF CIRCUITS (N) VS MESSAGE RATE & MESSAGE DURATION FOR P(<0.25 SEC) = 0.10, DWELL TIME t_d (SEC) FOR CIRCUIT SWITCH

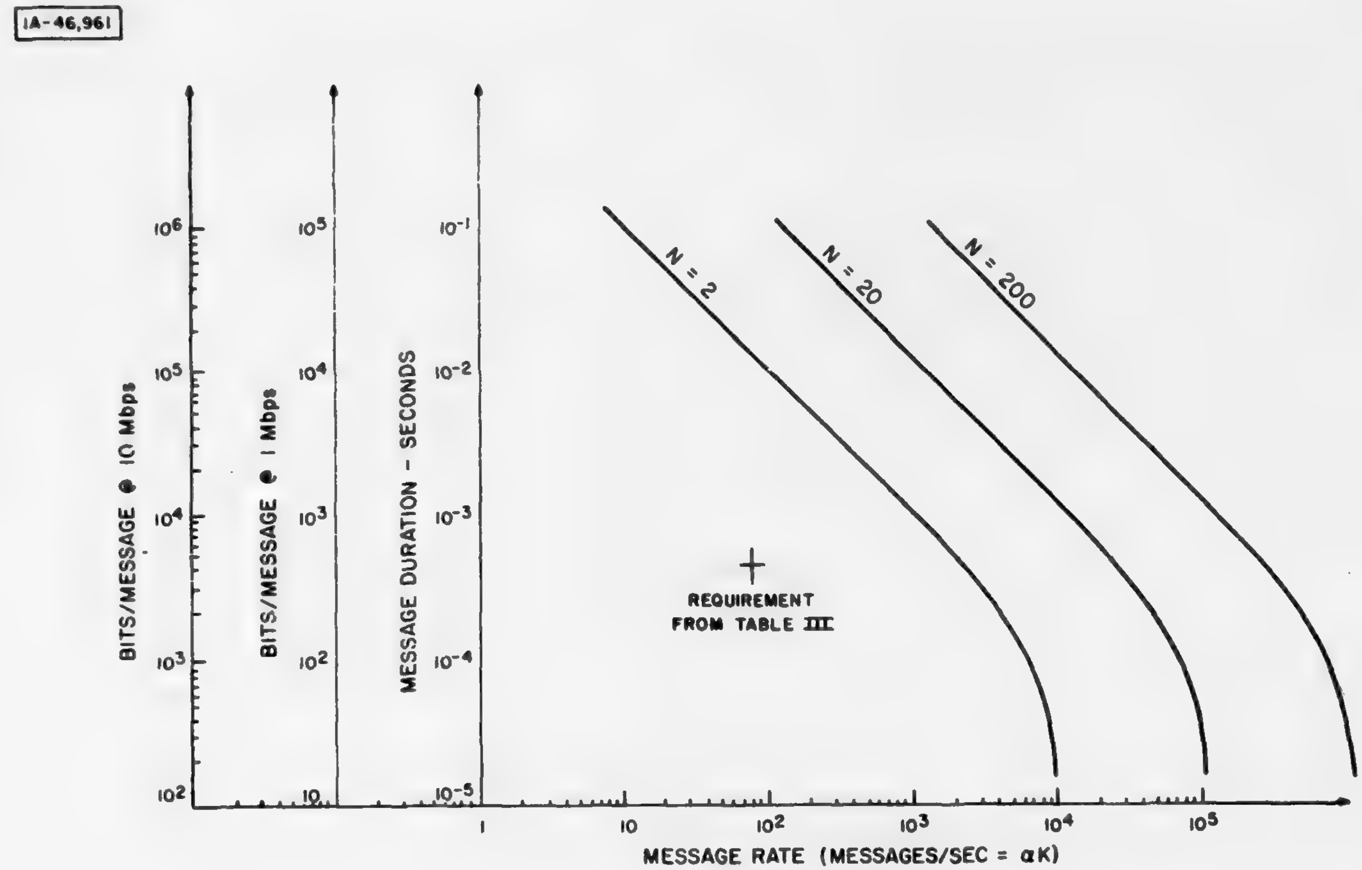

Figure 16 QUANTITY OF CIRCUITS (N) VS MESSAGE RATE & MESSAGE DURATION FOR P(<.01 SEC) = 0.10; DWELL TIME (t_d) = 10^{-4} SEC FOR CIRCUIT SWITCH

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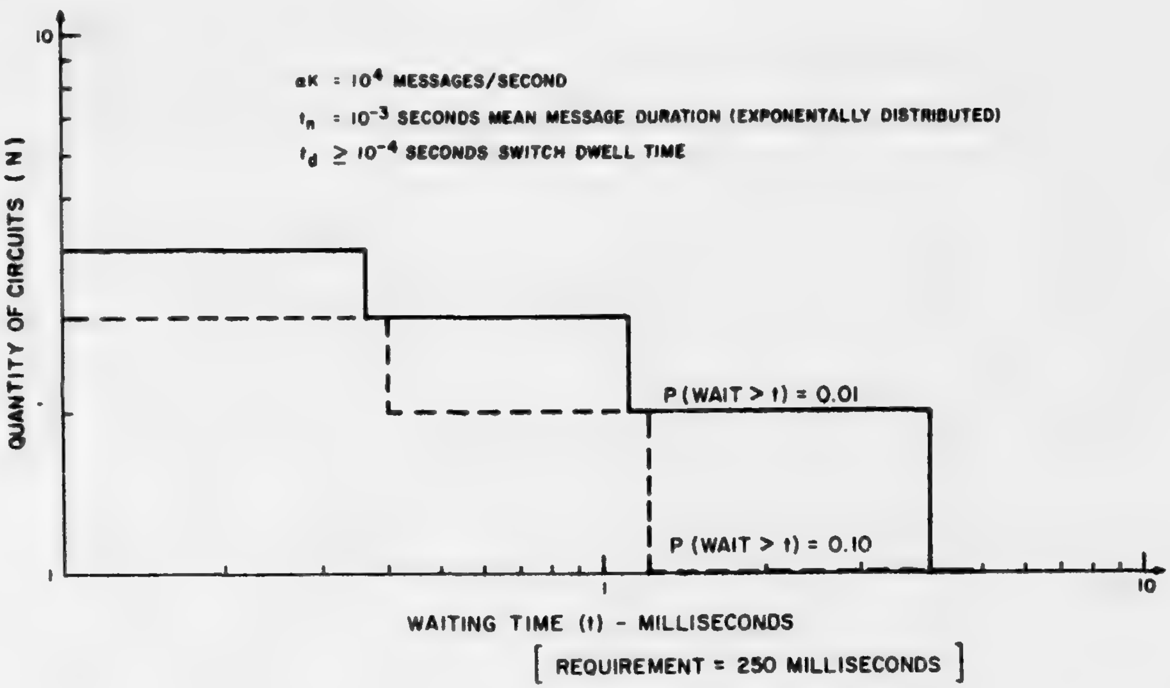

Figure 17 QUANTITY OF CIRCUITS (N) VS ACCESS TIME (t) AND PROBABILITY P(>t) OF WAITING TIME EXCEEDING t FOR CIRCUIT SWITCH

1A-46,963

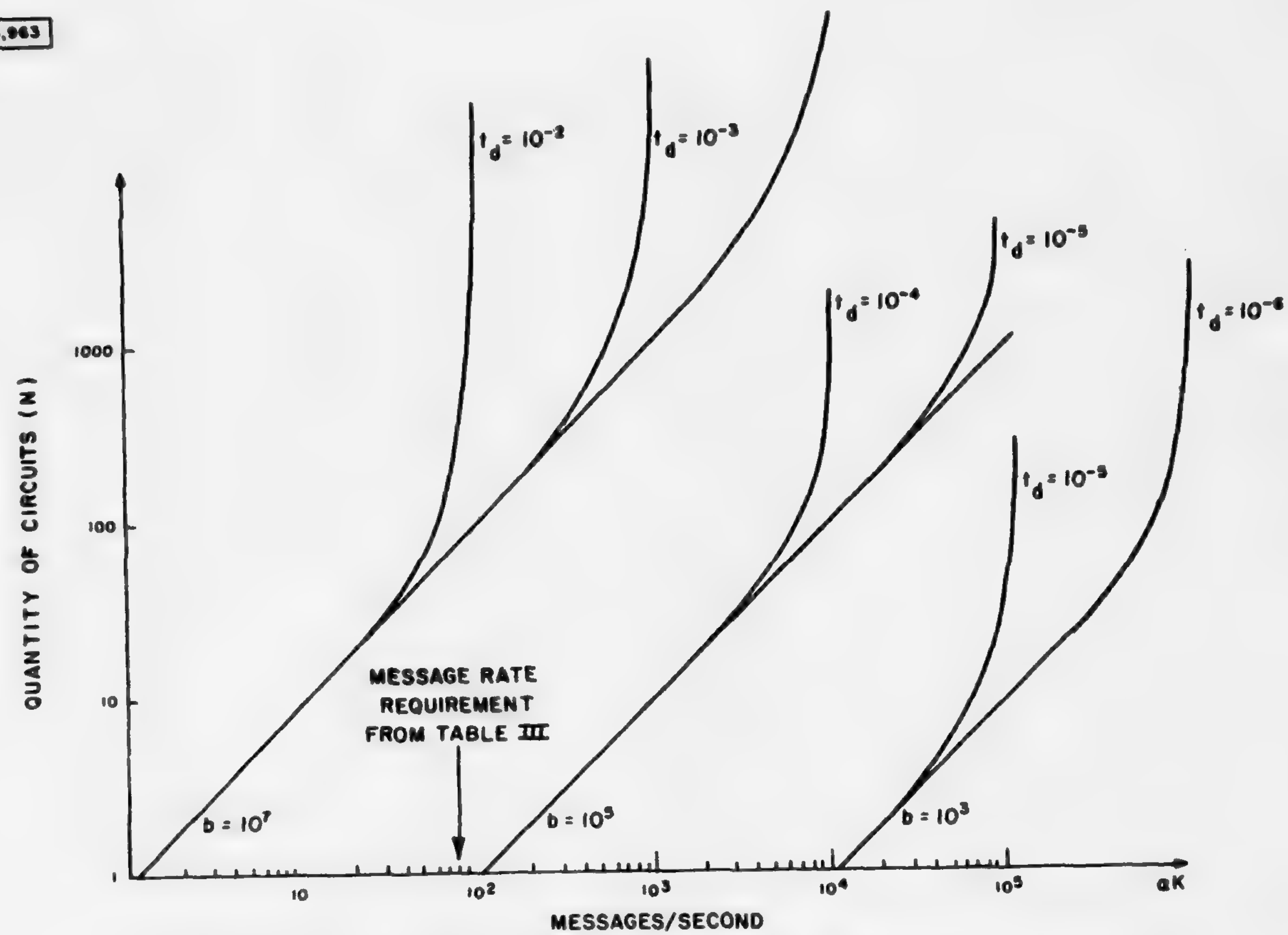

Figure 18 QUANTITY OF CIRCUITS (N) VS MESSAGE RATE (αK) & t_d
(ASSUMES 10 Mbps OPERATION)

Device Type	αK(Messages per Second)	bαK (Bits per Second)
Terminals	10	10,000
External Communications (Input)	30	6,840
Mass Storage to Computer	.1	100,000
Computer to Terminals	10	100,000
Computer to External Communications	30	6,840
Computer to Mass Storage	.1	100,000
	80.2	323,680

This results in an average message length of 4035 bits. Referring to Figure 15, for a message rate of 80.2 messages per second, a single circuit switch can support an average message length of 11,000 bits at one Mbps. Therefore, the assumed requirements are easily supported by a single one Mbps switch.

MESSAGE SWITCHING

The capacity required in a message switch depends upon the processing time required per message and the message rate throughput. The processing time per message is weakly dependent upon the number of subscribers involved in the network and upon the message length. However, to a first approximation, these may be considered as constants. Figure 19 shows the approximate dependence of capacity (number of parallel message switching devices required) upon processing (throughput time per message), message length (b), message arrival rate per subscriber (α), and number of subscribers (K).

t_s is the time required for the message switch computer to process a single message, that is, transfer it from input buffer to output buffer. For a message switching computer operating with a two microsecond average instruction cycle (a conservative figure), and executing 100 instructions per message processed (also conservative), t_s would be 2×10^{-4} seconds. The total throughput time is the sum of three elements: input buffering time while the message awaits processing, processing time t_s, and output buffering time. Queuing time in the input buffer is on the order of milliseconds; analysis identical to that presented for circuit switch queuing applies. Output buffering

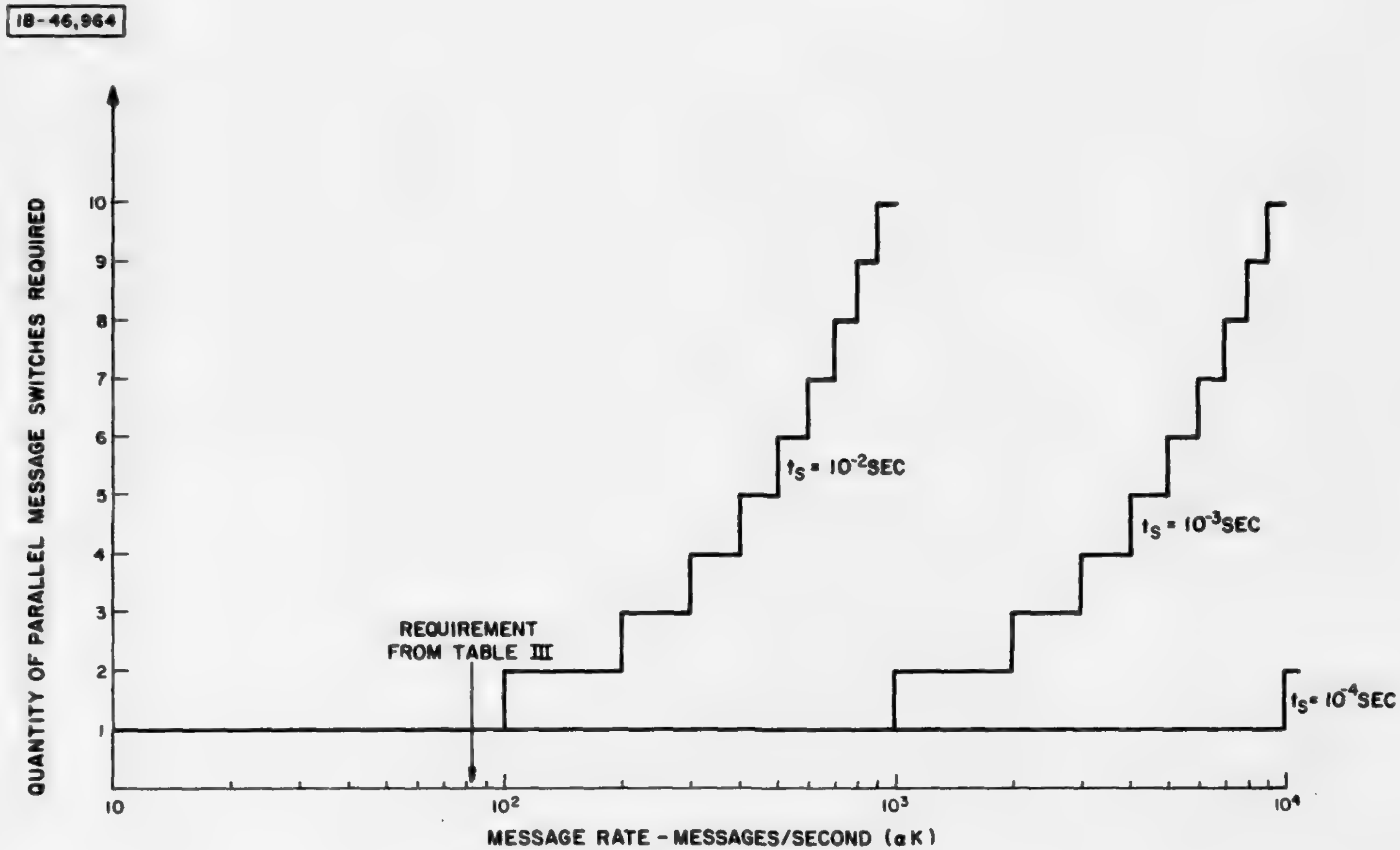

Figure 19 QUANTITY OF PARALLEL MESSAGE SWITCHES VS MESSAGE RATE (αK) AND MESSAGE PROCESSING TIME (t_S)

time is equal to the time required for a multiplexer to cycle to the appropriate receive address and output the message. For a multiplexer operating at typical computer channel rates, this time is much less than a second for messages of lengths typical of console operations.

Thus, the number of message switching devices needed is one for the stated requirements, or at most, two for plausible increases in this traffic load.

CONTENTION BUS

The capacity available from a contention bus scheme depends upon the message traffic in bits per second. This may be considered as the product of the number of subscribers (K), the message transmission rate per subscriber (α) and the mean message length per subscriber (b). The dependence of capacity on the product of these parameters is shown in Figure 20. The assumption is made that the average message length is long as compared to a slot length, so that inefficiency due to incomplete filling of slots is not significant. With this assumption, there is a difference of approximately a factor of two between the performance of a slotted contention system and an unslotted contention system. This is described in Appendix A. If the slotted contention bus efficiency is significantly reduced by the common occurrence of partially filled slots, the slot length is inappropriate. If this occurs because the standard deviation of message lengths is large compared to the mean message length, the unslotted contention bus may be preferable. The crossover occurs when the slot utilization is 50 percent or less.

The access time is determined by the probable number of retransmissions required for the message, which is a function of the bus loading, and the delay between retries to transmit the message. For a bus operating at one Mbps or more, and supporting the requirements stated in Table III, the average delay to transmit a single message is on the order of milliseconds at full capacity, indicating that response time is not a significant problem for the contention bus.

STATIC DEDICATED ASSIGNMENT BUS

The usable capacity of a static dedicated assignment bus depends upon the number of terminals to which capacity is allocated, the capacity allocation to each terminal, and the required overhead for bus control and monitoring. The capacity required is thus independent of the actual traffic statistics. This differs from the other approaches. Capacity is determined strictly by the number of terminals and their burst transmission rates. The resulting capacity requirement, as a function of the number of terminals provided service is shown in Figure 21. A service rate of 300 bits per second transmitted per

IA-46,965

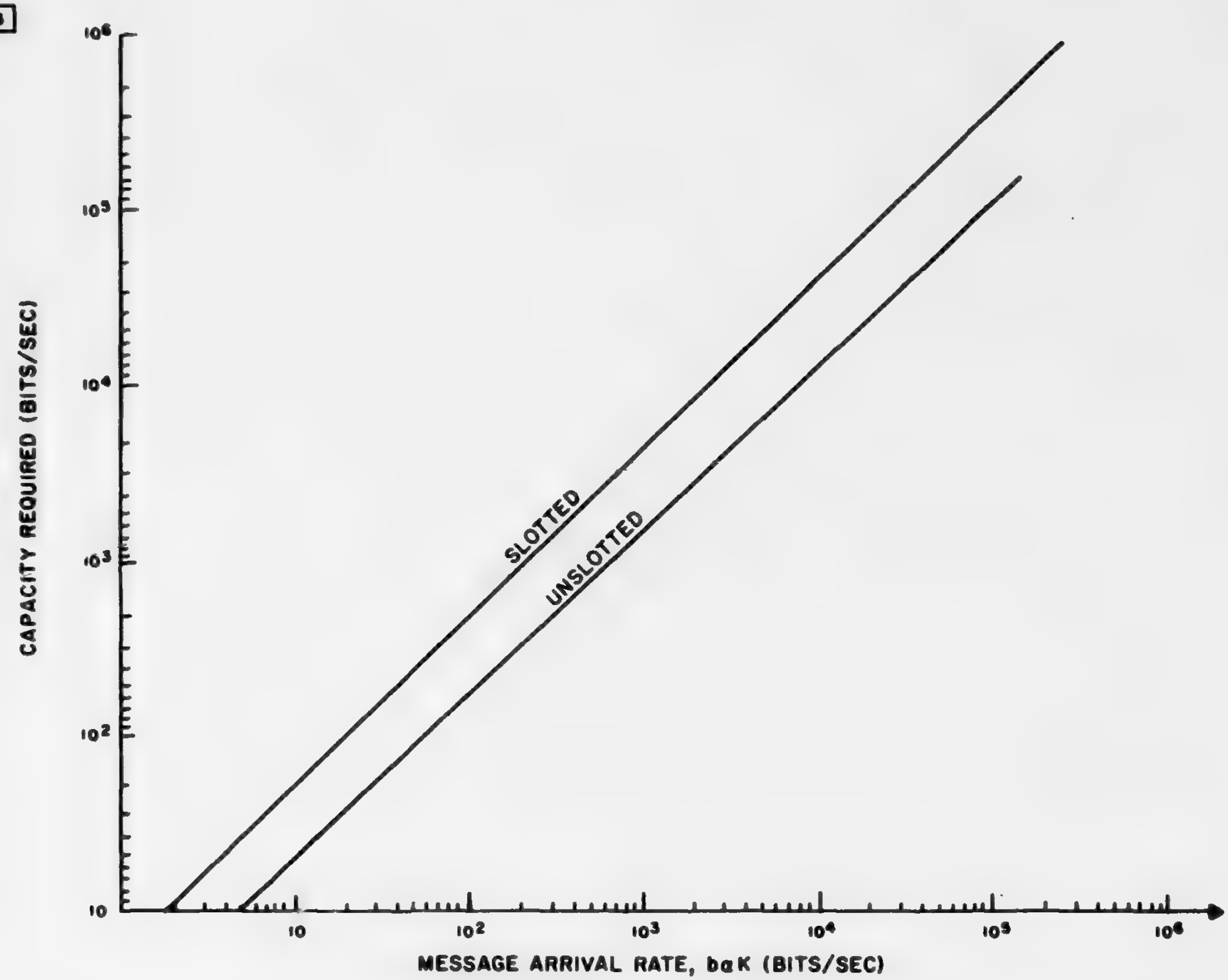

Figure 20. CONTENTION BUS CAPACITY COMPARISON

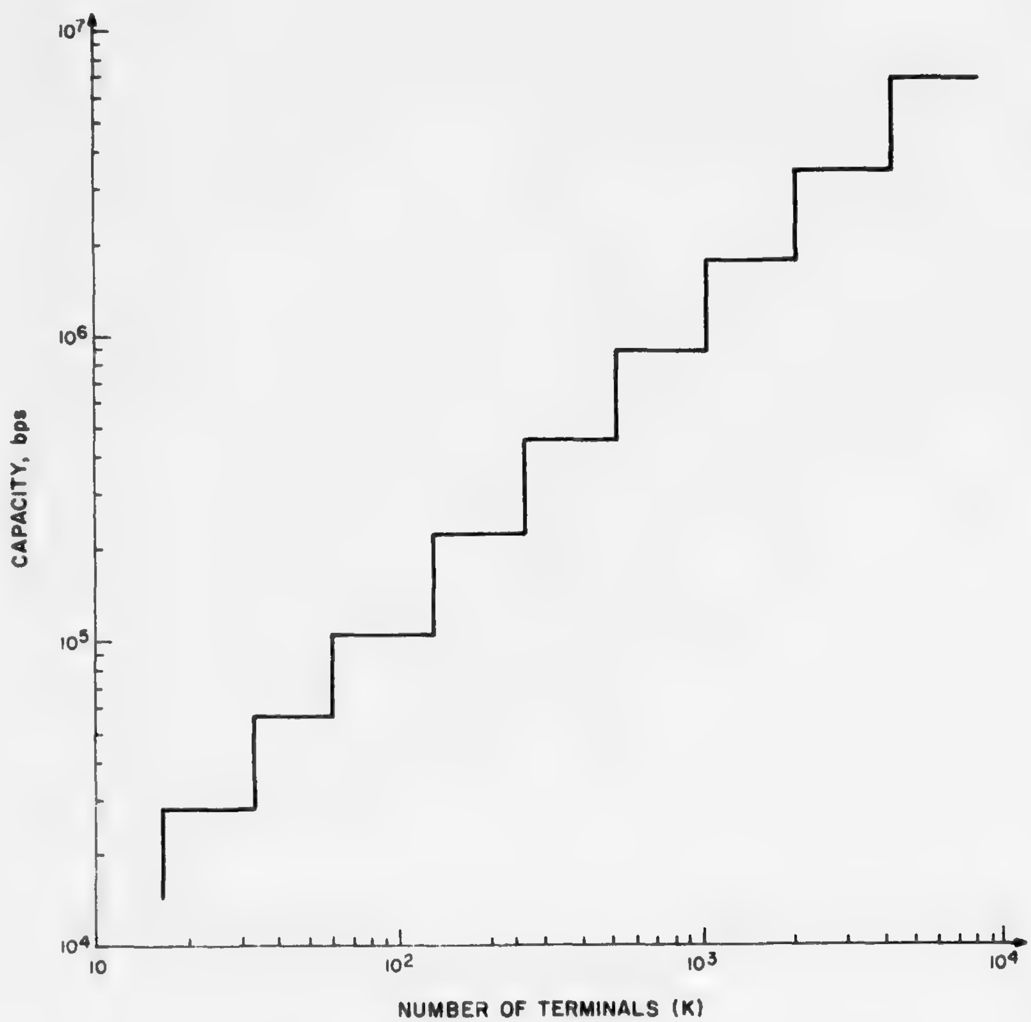

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Figure 21. DEDICATED ASSIGNMENT BUS CAPACITY VS NO. TERMINALS K
GIVEN 300 bps/TERMINAL, 10% COMPUTER ALLOCATION,
1 SLOT/FRAME/TERMINAL FOR TECH CONTROL

subscriber and an allocation to a central computer equal to ten percent of the total allocation to terminals is assumed. This assumption is supported by Figure 30 of Appendix C and associated discussion.

The response time provided by the static dedicated assignment bus is determined by the interval between slots assigned to the lowest data rate devices on the bus. Assume that a slot contains 256 data bits and 128 overhead bits, and that a frame is .85 seconds long. The minimum subscriber assignment of one slot per frame corresponds to 300 bits per second and the mean delay for a one-slot frame assignment is 0.426 seconds. This time can be reduced by increasing capacity, and the reduction is in proportion to the increased capacity as shown in Figure 22. The response time delivered to higher data rate devices, at any given total capacity, is proportional to the data rate of service provided.

DYNAMIC DEDICATED ASSIGNMENT BUS

The dynamic dedicated assignment bus uses the capacity more efficiently than the static dedicated assignment bus. This is accomplished by time-sharing a set of assignments among a group of subscribers. Slot assignments are provided to subscribers only when they have data to transmit. When the transmission is completed, the assignment is relinquished.

The ratio of subscribers to assignments will be greater than one. This ratio is limited by the subscriber message statistics. If messages are short with low duty cycles, the ratio may be large. As the duty cycle increases, the ratio must be kept low. In the limiting case, where all subscribers transmit continuously, the ratio must be unity; this degenerate case is identical to a static dedicated assignment bus.

POLLED BUS

The capacity required by a polled bus is equal to the sum of the capacity needed to transfer the data plus the capacity required to perform the controller-to-subscriber interchanges of polling messages. The time required for the latter function depends upon the physical length of the network because of the propagation delay involved. However, for network lengths likely to be encountered in a tactical operating center environment (considerably less than one mile or .28 microseconds propagation delay), the propagation delay is minor compared to the processing delay involved in the polling interchange. The capacity required to support a given traffic load is plotted in Figure 23 as a function of the total information throughput rate (bαK). The

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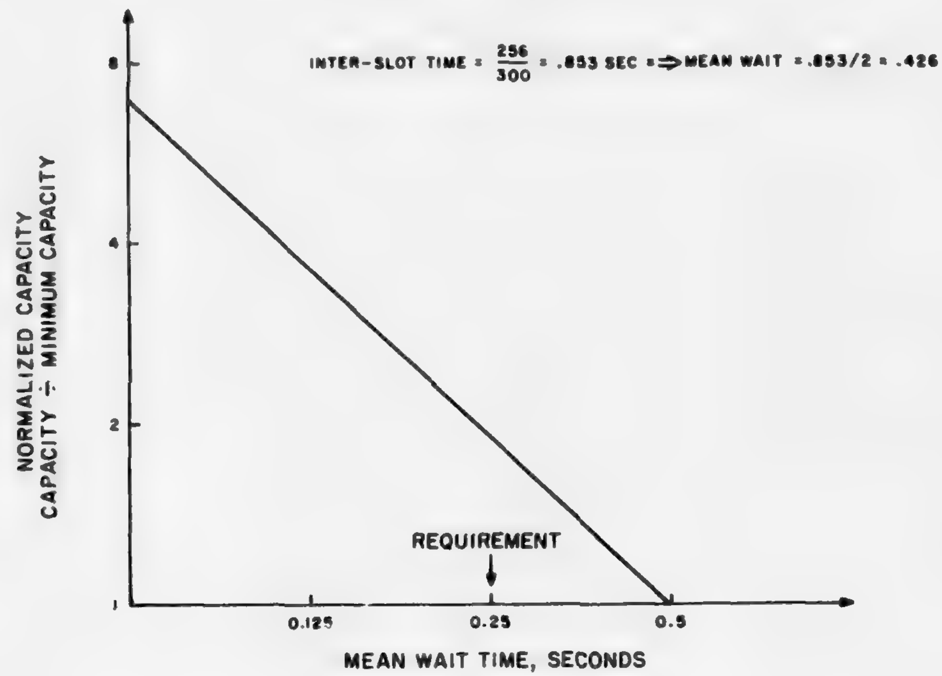

Figure 22 RESPONSE TIME - DEDICATED ASSIGNMENT BUS
ASSUME 300 bps TERMINALS @ 1 SLOT/FRAME

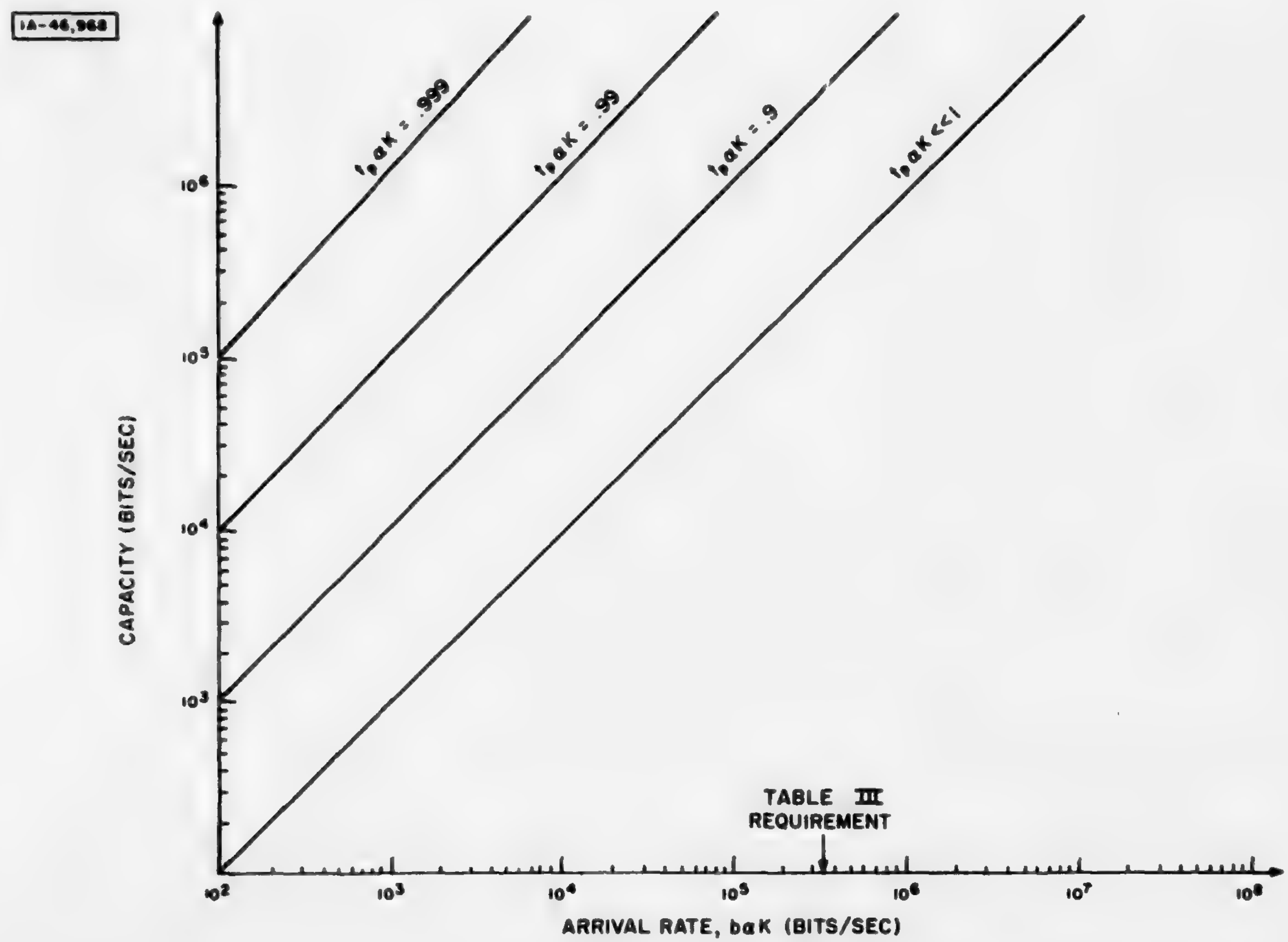

Figure 23 POLLED OR LOANED BUS CAPACITY

parameter $t_p \alpha K$ represents total overhead time. The normalized capacity (total bus capacity divided by mean message length (b)) is plotted in Figure 24 as a function of the message rate in messages per second received from all subscribers.

The polling time parameter (t_p) depends upon the bit rate, the physical size of the network (that is, propagation delay), and the number of bits in the polling message. Given a one Mbps bit rate, 2,000 feet round-trip distance, and 32 bits per polling message: t_p is on the order of 35 microseconds, and $t_p \alpha K$ equals 2.79×10^{-3}. This indicates that a one Mbps bus is more than adequate.

The access time delivered by a polled bus is determined by the number of active subscribers because the system must cycle through all transmitting subscribers in sequence. The improvement in access time achievable by increasing capacity is shown in Figure 25. Again, one Mbps capacity meets the .25 second requirement easily.

LOANED BUS

The performance of the loaned bus is mathematically similar to that for the polled bus. The difference arises because overhead time (time required between data transmission by different subscribers) is no longer a function of network size and tends to be a much smaller quantity. This overhead is needed only for a guard period to prevent overlap between messages from different subscribers. The message interchange required to establish which subscriber shall transmit next is accomplished on a separate frequency channel. Thus, the same curves shown in Figures 23, 24, and 25 apply, but lower levels of t_p are likely.

CONCLUSIONS REGARDING BUS PERFORMANCE

The material presented above demonstrates that any of the alternatives considered is technically capable of meeting the range of performance requirements anticipated for Modular C^3 Centers. In particular, any of the alternatives can meet the capacity requirements listed in Table III.

The relative performance limits of the different bus approaches are shown in Figure 26 as a function of the number of consoles and computers involved. Figure 26 compares the information transfer capability for the various capacity allocation strategies, indicating the number of terminal devices (K_T) and computers (K_C) which can be supported simultaneously. The traffic load imposed by these two classes of devices requires a bus burst transmission rate of 7.37 Mbps.

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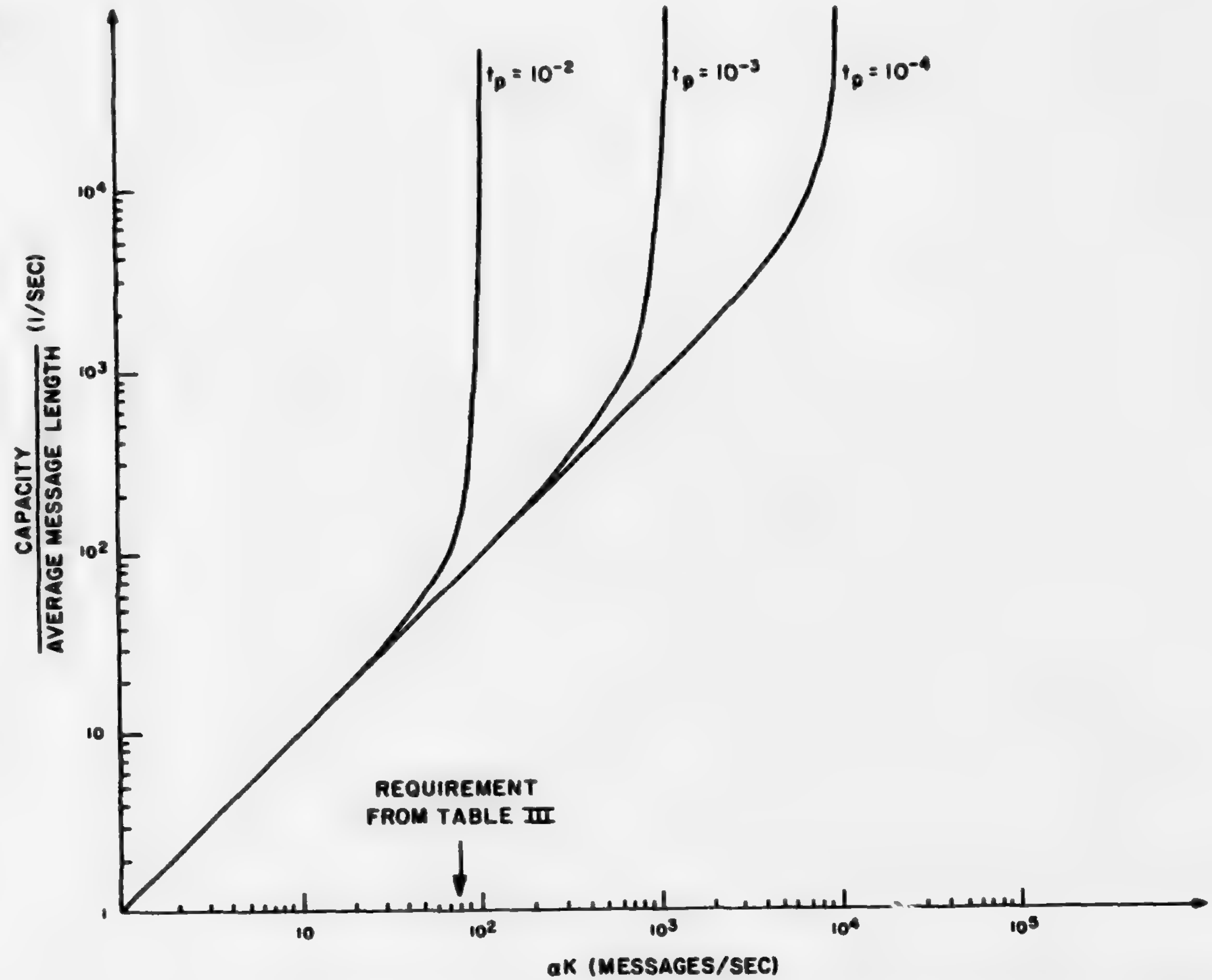

Figure 24 POLLED OR LOANED BUS NORMALIZED CAPACITY

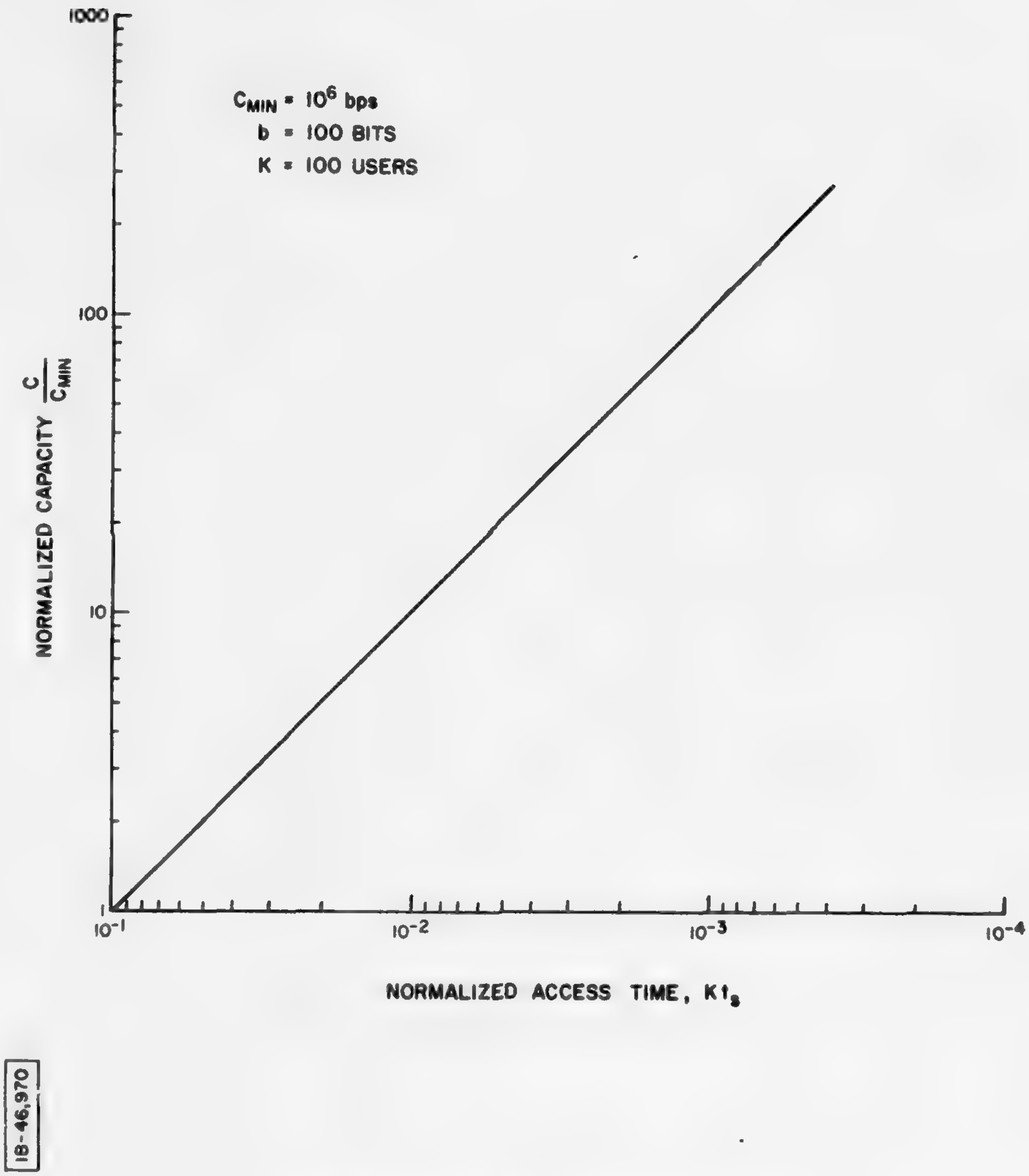

Figure 25 ACCESS TIME FOR A POLLED BUS

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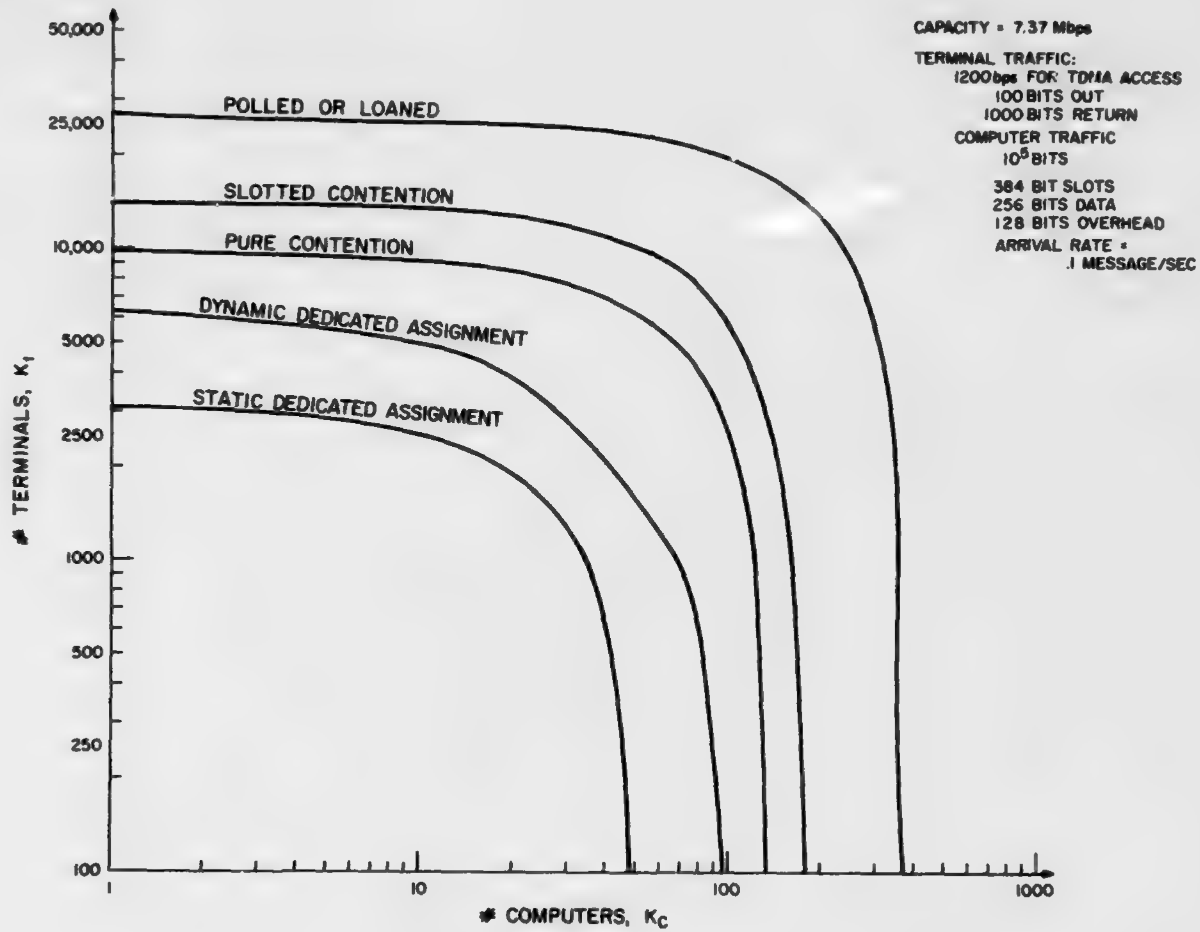

Figure 26 GROWTH POTENTIAL – COMPARISON OF BUS ALTERNATIVES

SECTION IV. PROCUREMENT COST

INTRODUCTION

This section discusses estimates of procurement cost comparisons for the eight interconnect alternatives being considered, assuming government procurement of militarized equipment from industry. Costs are divided into non-recurring (development) and recurring (unit production) categories. The non-recurring costs are those associated with the system development. Thus, they will be experienced only once and may be amortized over the total number of systems built. The recurring costs are those for building an individual system, excluding development. The total cost of the system is the recurring costs plus the proportionate share of the non-recurring costs. The following paragraphs elaborate on the information presented in Table IV, Cost Summary.

NON-RECURRING COSTS

The non-recurring costs are shown in the left-hand side of Table IV. These figures indicate the engineering design costs associated with each of the components of the network.

Network Control Computer

The non-recurring costs associated with the network control computer are the design of the control panel and operator interface hardware, and the programming and software design effort. The control panel design requires approximately a three man-month effort. Programming and software design estimates are based upon a cost of \$37.50 per line of executable assembler code (Reference 2). The software sizing estimates, shown in Table V, were derived on the basis of experience with similar functions.

Data Bus Repeater

The data bus repeater is required only for the bus interconnect alternatives. The design of the physical packaging for this unit requires a three man-month effort. The power supply is an off-the-shelf item. The modem design will require four-fifths of a man-year and the logic design is anticipated to be a one man-year effort. Manning costs are estimated on the basis of \$50,000 per engineering man-year.

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TABLE IV

COST SUMMARY

COMPONENT	NONRECURRING COSTS							
	STATIC CKT SWITCH	DYNAMIC CKT SWITCH	MESSAGE SWITCH	CONTENTION BUS	STATIC TDMA BUS	DYNAMIC TDMA BUS	POLLED BUS	LOANED BUS
BUS CONTROL								
Element								
Minicomputer								
Control Panel & Operator Inter H/W	10,000	10,000	10,000	10,000	10,000	10,000	10,000	10,000
Prog. & S/W Design	159,000	230,000	244,000	246,000	230,000	259,000	251,000	253,000
BUS REPEATER								
Boxes, Connectors				10,000	10,000	10,000	10,000	10,000
Power Supply								
Modem				40,000	40,000	40,000	40,000	40,000
Logic				50,000	50,000	50,000	50,000	50,000
Assembly & Test (Production)								
CABLE NETWORK								
Design	50,000	50,000	50,000	50,000	50,000	50,000	50,000	50,000
Dual Cable								
-Amplifiers								
SUBSCRIBER INTERFACE UNIT								
Box, Connectors	10,000	10,000	10,000	10,000	10,000	10,000	10,000	10,000
Cable Tap								
Power Supplies								
Logic	10,000	50,000	30,000	50,000	50,000	50,000	50,000	50,000
Modem	40,000	40,000	40,000					
Microprocessor Programming (Excluding S/W Development Facility)		25,000		50,000	50,000	50,000	50,000	50,000
SIU Design/Integration	100,000	100,000	100,000	100,000	100,000	100,000	100,000	100,000
SIU Assembly & Test (Production)								
BUFFER/MULTIPLEXOR UNIT								
Boxes, Connectors, Internal Cabling		25,000	25,000					
Power Supply								
CP Interface & MUX Logic Control		50,000	50,000					
Subscriber Interface Controllers								
Design/Integration		100,000	100,000					
Assembly Test								
Modem								
SWITCHING ASSEMBLY								
Boxes, Connectors	20,000	20,000						
Power Supply								
Block Switching Matrices	100,000	100,000						
Modem								
Computer Interface	50,000	50,000						
SUBTOTAL	549,000	860,000	659,000	616,000	600,000	629,000	621,000	623,000
Risk Allowance 50%	274,500	430,000	329,500	308,000	300,000	314,500	310,500	311,500
TOTAL	823,500	1,290,000	988,500	924,000	900,000	943,500	931,300	934,500

TABLE IV (Continued)

COMPONENT	RECURRING COSTS							
	STATIC CKT SWITCH	DYNAMIC CKT SWITCH	MESSAGE SWITCH	CONTENTION BUS	STATIC DED. ASSIGN.	DYNAMIC DED. ASSIGN.	POLLED BUS	LOANED BUS
NETWORK CONTROL								
Element								
Minicomputer	8,000	10,000	12,500	12,500	12,500	12,500	12,500	12,500
Control Panel & Operator Inter H/W	3,000	3,000	3,000	3,000	3,000	3,000	3,000	3,000
Prog. & S/W Design								
BUS REPEATER								
Boxes, Connectors				100	100	100	100	100
Power Supply				50	50	50	50	50
Modem				200	200	200	200	200
Logic				1,000	1,000	1,000	1,000	1,000
Assembly & Test (Production)				350	350	350	350	350
CABLE NETWORK								
Design								
Dual Cable	1,800	1,800	1,800	720	720	720	720	720
-Amplifiers	3,150	3,150	3,150	2,100	2,100	2,100	2,100	2,100
SUBSCRIBER INTERFACE UNIT								
Box, Connectors	100N	100N	100N	100N	100N	100N	100N	100N
Cable Tap	30N	30N	30N	7.5N	7.5N	7.5N	7.5N	7.5N
Power Supplies	50N	50N	50N	50N	50N	50N	50N	50N
Logic	100N	700N	300N	700N	700N	700N	700N	700N
Modem	200N	200N	200N	200N	200N	200N	200N	400N
Microprocessor Programming (Excluding S/W Development Facility)								
SIU Design/Integration								
SIU Assembly & Test (Production)	200N	250N	250N	250N	250N	250N	250N	250N
BUFFER/MULTIPLEXER UNIT								
Boxes, Connectors, Internal Cabling		1,000	1,000					
Power Supply		50	50					
CP Interface & MUX Logic Control		1,000	1,000					
Subscriber Interface Controllers		500	500					
Design/Integration		1,000	1,000					
Assembly Test		250	250					
Modem			200N					
SWITCHING ASSEMBLY								
Boxes, Connectors	500	500						
Power Supply	50	50						
Block Switching** Matrices	60N	60N						
Modem	200N	200N						
Computer Interface	1,000	1,000						
TOTAL*	17,500+	23,300+	24,250+	20,020+	20,020+	20,020+	20,020+	20,020+
	940N	1590N	1130N	1307.50N	1307.50N	1307.50N	1307.50N	1307.50N

*N = the number of subscribers in the system

** The number of 8-port switching modules required for a unidirectional 3-stage, conditionally nonblocking switching matrix was approximated to be 0.6 modules per subscriber at a cost per module of $100.

TABLE V
SOFTWARE ESTIMATES
(16 bit words)

FUNCTION	STATIC CKT SWITCH	DYNAMIC CKT SWITCH	MESSAGE SWITCH	CONTENTION	STATIC DED. ASSIGN	DYNAMIC DED. ASSIGN	POLLED	LOANED
EXECUTIVE	3000	3500	3500	3500	3500	3500	3500	3500
INITIALIZATION	300	300	200	200	300	300	200	200
CONSOLE ROUTINE	750	1000	1000	1000	1000	1000	1000	1000
OPERATION CONTROL	----	300	300	300	300	300	500	500
STATUS ROUTINE	----	500	500	500	500	500	500	500
TECH CONTROL	----	100	100	100	100	100	100	100
REQUEST HANDLER	----	250	500	750	250	1000	500	750
POLLING ROUTINE	----	----	----	----	----	----	200	----
DATA FILTER ROUTINE	----	200	----	----	----	----	----	----
MESSAGE FORMAT ROUTINE	200	200	200	200	200	200	200	200
SUBTOTAL	4250	6350	6300	6550	6150	6900	6700	6750
TABLES & BUFFERS	1000	1000	5000	2000	2500	2500	2500	3000
OPERATING SYSTEM	1500	1500	1500	1500	1500	1500	1500	1500
SUBTOTAL	6750	8850	12800	10050	10150	10900	10700	11250
RISK ALLOWANCE (25%)	1675	2212	3200	2500	2550	2725	2675	2800
TOTAL	8425	11062	16000	12550	12700	13625	13375	14050
SUGGESTED CORE	8K	12K	16K	16K	16K	16K	16K	16K

Cable Network

Each of the alternatives under consideration requires the design and layout of a cable plant which will connect the computer to the subscriber terminals. A reasonable effort for this task is one man-year.

Subscriber Interface Unit

Each of the alternatives being considered requires some form of subscriber interface unit. In each case, the design of the physical packaging will require approximately a three man-month effort. The power supplies are assumed to be off-the-shelf models. The logic for the various alternatives will vary in proportion to the complexity of the interface unit. The comparison of complexities between the various units is presented in Section II. It is shown there that the static circuit switch interface unit is significantly less complex than any of the other alternatives and that the message switch is somewhat less complex than the remaining alternatives. All of the bus alternatives and the dynamic circuit switch are of comparable complexity.

The modem design for the static circuit switch, dynamic circuit switch, and the message switch require a one man-year effort. For the bus alternatives, the subscriber interface unit will use the modem that was used in the data bus repeater. Thus, the non-recurring costs associated with the development of the modem have already been considered.

The more complex subscriber interface units will require microprocessor programming. All of the bus alternatives are approximately of equal complexity. The dynamic circuit switch microprocessor programming will be less complex and, therefore, will require a six man-month programming effort.

The task of specifying the functions of each component in the subscriber interface unit and interfacing between these components is entitled "The Subscriber Interface Unit Design/Integration Effort." This task will require approximately two man-years.

Buffer/Multiplexer Unit

The dynamic circuit switch and the message switch alternatives require a buffer-multiplexer unit to route messages. Since the boxes, connector, and internal cabling for this unit are significantly more complex than for the subscriber interface unit, it is assumed that this will require approximately a six man-month effort for design.

The power supplies are off-the-shelf. The control processor interface and multiplexer logic control design are a one man-year effort and the design/integration is a two man-year effort.

Switching Assembly

The circuit switch alternatives require a switching assembly to connect/disconnect subscribers as commanded, report status, and support diagnostics. A six man-month effort will be required to design the boxes and connectors for this device. The power supply is to be purchased off-the-shelf.

A solid-state block-switching matrix, similar to the one designed by Sperry, Univac (Reference 1) can be developed with approximately a two man-year effort.

In addition, a one man-year effort would be required to design the computer interface for the circuit switch alternatives.

Summary of Non-Recurring Costs

The subtotal in Table IV shows the estimate of non-recurring costs. A 50% risk allowance is added to cover contingencies, plus such items as production tooling, administrative overhead, and cost of capital. This leads to the total non-recurring costs presented in Table IV. The non-recurring costs are presented graphically in Figure 27. Costs vary between $823,500 for the static circuit switch and $1,290,000 for the dynamic circuit switch interconnect. The bar graph, in Figure 27, clearly demonstrates the relative, non-recurring costs of the various interconnects. The bus alternatives are all within a narrow range around $920,000; the message switch is of comparable cost to the buses; the dynamic circuit switch is more expensive; and the static circuit switch is less expensive.

RECURRING COSTS

Network Control Computer

The recurring costs for the network control computer in Table IV are for the control computer and the operator console. The console costs approximately $3,000 for each of the alternatives. The computer

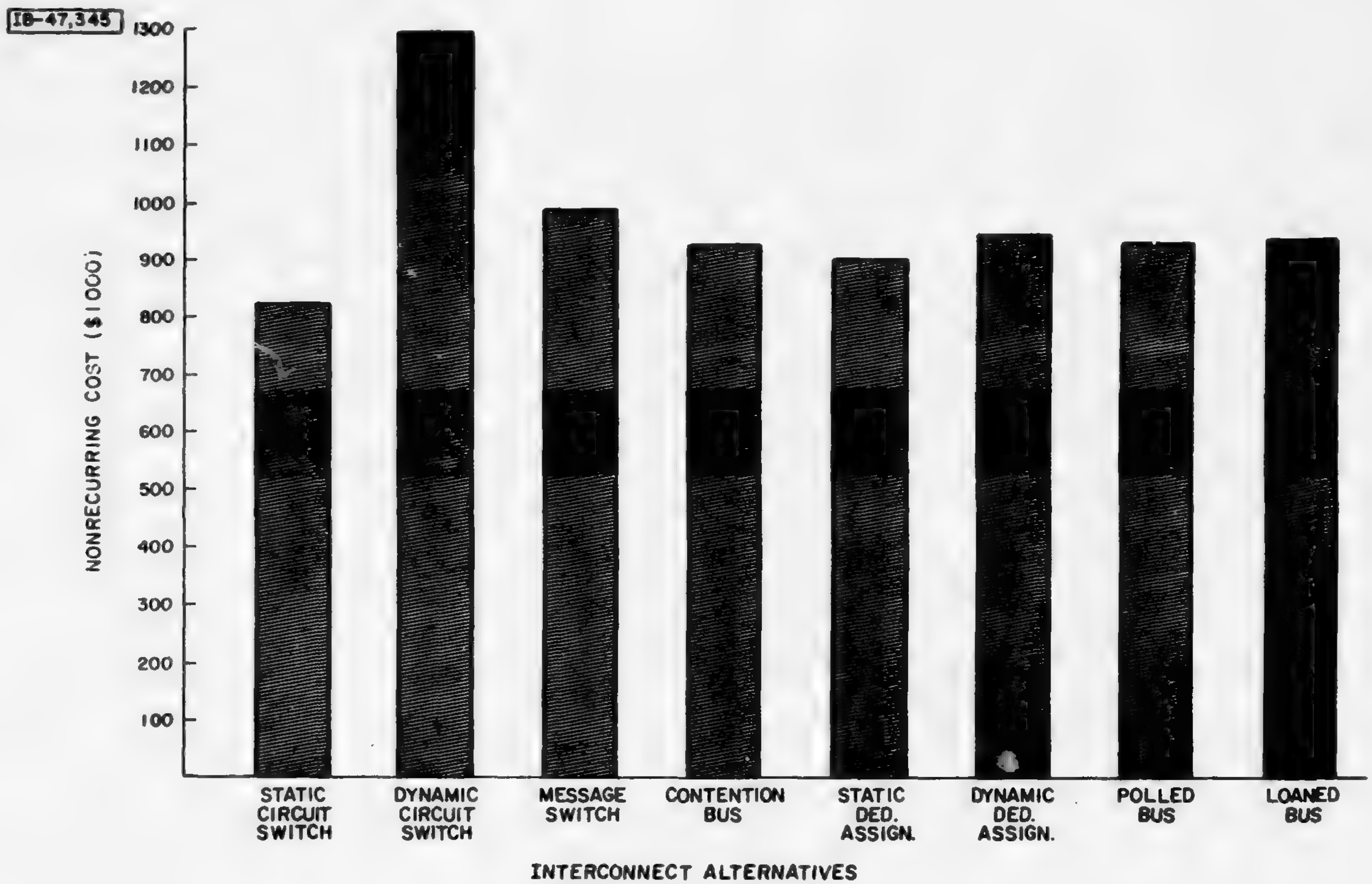

Figure 27. NON-RECURRING COSTS OF THE INTERCONNECT ALTERNATIVES

cost is a function of the storage required to support the control functions. The detailed breakdown, which supports the costing, is presented in Section II.

Data Bus Repeater

Each of the data bus alternatives requires a data bus repeater. The costs shown in Table IV indicate the cost of hardware and assembly for this unit. These amounts are based on experience from the MITRIX Project.

Cable Network

The recurring costs for the network shown in Table IV are for the physical installation of the cable. The cost of installing cable is in proportion to the length of the cable. For the circuit switch and message switch alternatives, the length is assumed to be 4,500 feet. The circuit and message switch alternatives require point-to-point connections between the switch and all subscribers, while the bus alternatives require only a common connection for all subscribers. Therefore, the cable length for the bus alternatives was assumed to be 1800 feet. Using a cost of $.40 per foot for coaxial cable, cable costs are $1800 for the circuit and message switch alternatives and $720 for the buses. Assuming six amplifiers for the circuit and message switch cases and four amplifiers for the bus, the total cost of amplifiers (at $525 each) is $3,150 and $2,100, respectively. The cable lengths were estimated by assuming 100 terminals, each occupying a six-foot square enclosure.

Subscriber Interface Unit

The SIU is expected to be less than one cubic foot in volume for all the alternatives. It will have two cable connectors, one power connector, one pilot light and one power switch, but no other controls. A $100 unit cost was assumed for the box controls and connectors. The use of standard CATV taps and an off-the-shelf power supply were assumed.

All the approaches require control logic, although it differs in complexity among the alternatives. In all cases, use of a microprocessor (Intel 8080 or equivalent) with appropriate support circuitry is assumed. In addition, the bus alternatives require custom LSI circuitry to perform high-speed bus control functions. The dynamic circuit switch and message switch require a lesser mount of LSI. It was conservatively estimated that five LSI chips are required for the bus and the dynamic circuit switch SIU, at $100 each (production cost). One LSI chip was assumed for the message switch. Use of a single-channel, frequency shift keyed (FSK) modem was assumed and $200 for hardware was estimated.

Buffer/Multiplexer Unit

The buffer/multiplexer unit shown in Table IV is required for the dynamic circuit switch and the message switch alternatives. It is assumed that the boxes, connectors, and internal cabling will cost $1,000 for each of these alternatives. The power supply will cost $50. The control processor interface and multiplexer logic control will cost $1,000. The subscriber interface controllers will cost $500. The design and integration effort will cost $1,000. The assembly and test will cost $250. Each of these alternatives requires one modem per subscriber. This cost is included in this section for the message switch alternative; however, it is included in the switching assembly section for the dynamic circuit switch alternative.

Switching Assembly

The static circuit switch and dynamic circuit switch alternatives require a switching assembly. The recurring costs associated with the switch assembly are $500 for the boxes and connectors, $50 for the power supplies, and $60 per subscriber for the block-switching matrices. This number is an approximation that has been derived from the Sperry information on their block-switching matrix. The modem required for the switching assembly costs $200 per subscriber, the computer interface costs $1,000.

Summary of Recurring Costs

The total shown in Table IV is the estimate of the recurring costs.

Recurring costs have two components. The first is a basic system cost. This covers the basic system components such as the network control element, data bus repeater, cable network, buffer/multiplexer unit and portions of the switching assembly. It can be seen that all bus interconnects have the same basic system costs. This is because they each require essentially the same fixed plant. The dynamic circuit switch and message switch interconnects require a buffer/multiplexer unit rather than a data bus repeater. This accounts for their additional expense. In addition, the static circuit switch interconnect can operate with a smaller computer and no buffer/multiplexer. Consequently, it has the lowest fixed costs of any of the alternatives.

The second component of the recurring costs is the per-subscriber cost. This is an estimate of the additional cost of adding a subscriber to the system. These costs are constant for all of the bus interconnect alternatives.

The message switch interconnect requires a modem to the buffer/multiplexer unit as well as a subscriber interface unit for each additional subscriber. However, its subscriber interface unit logic is significantly less complex than the logic in the bus subscriber interface unit. Consequently, the per-subscriber costs are less for the message switch interconnect than for the bus interconnect alternatives.

The dynamic circuit switch interconnect has the highest per-subscriber costs of any of the interconnect alternatives. This is because its subscriber interface unit logic is significantly more complex than any of the other units.

The combination of fixed and variable recurring costs is presented graphically in Figure 28.

TOTAL COST

The total costs for the interconnect alternatives are shown in Figure 29. In each case, the non-recurring costs are assumed to be shared among 100 systems. It can be seen that the intersections occur before ten subscribers. For systems with more than ten subscribers, the interconnects may be ranked in ascending order by recurring costs as follows: static circuit switch, message switch, bus alternatives, and dynamic circuit switch. The basic costs (for the interconnection plant, excluding subscriber interface units) are all within the range of $25,000 to $36,000. However, because the subscriber interface unit costs vary significantly, the total cost for a system with 100 subscribers varies between about $120,000 and $195,000. This indicates that the most important issue in the cost comparison is the subscriber interface unit cost.

The subscriber interface unit cost varies from $940 to $1,590. The key factor affecting SIU cost is the command capability. The static circuit switch SIU is the least complex. It has no command capabilities, and its cost is estimated to be $650. In contrast, the dynamic circuit switch does require a command capability. Since the more complex command functions require more elaborate logic, SIU cost increases to $1,300.

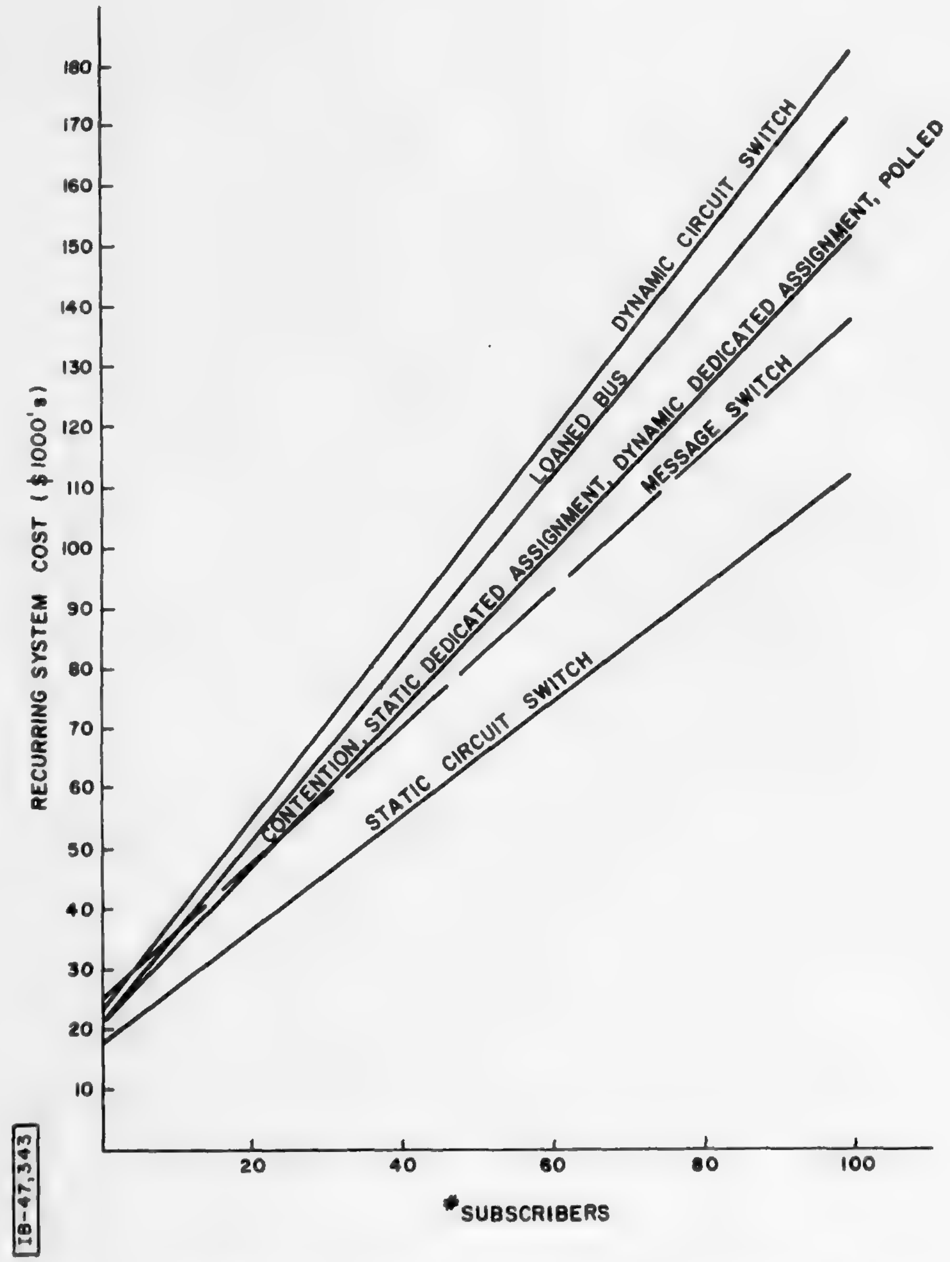

Figure 28. RECURRING COSTS FOR AN INTERCONNECT NETWORK

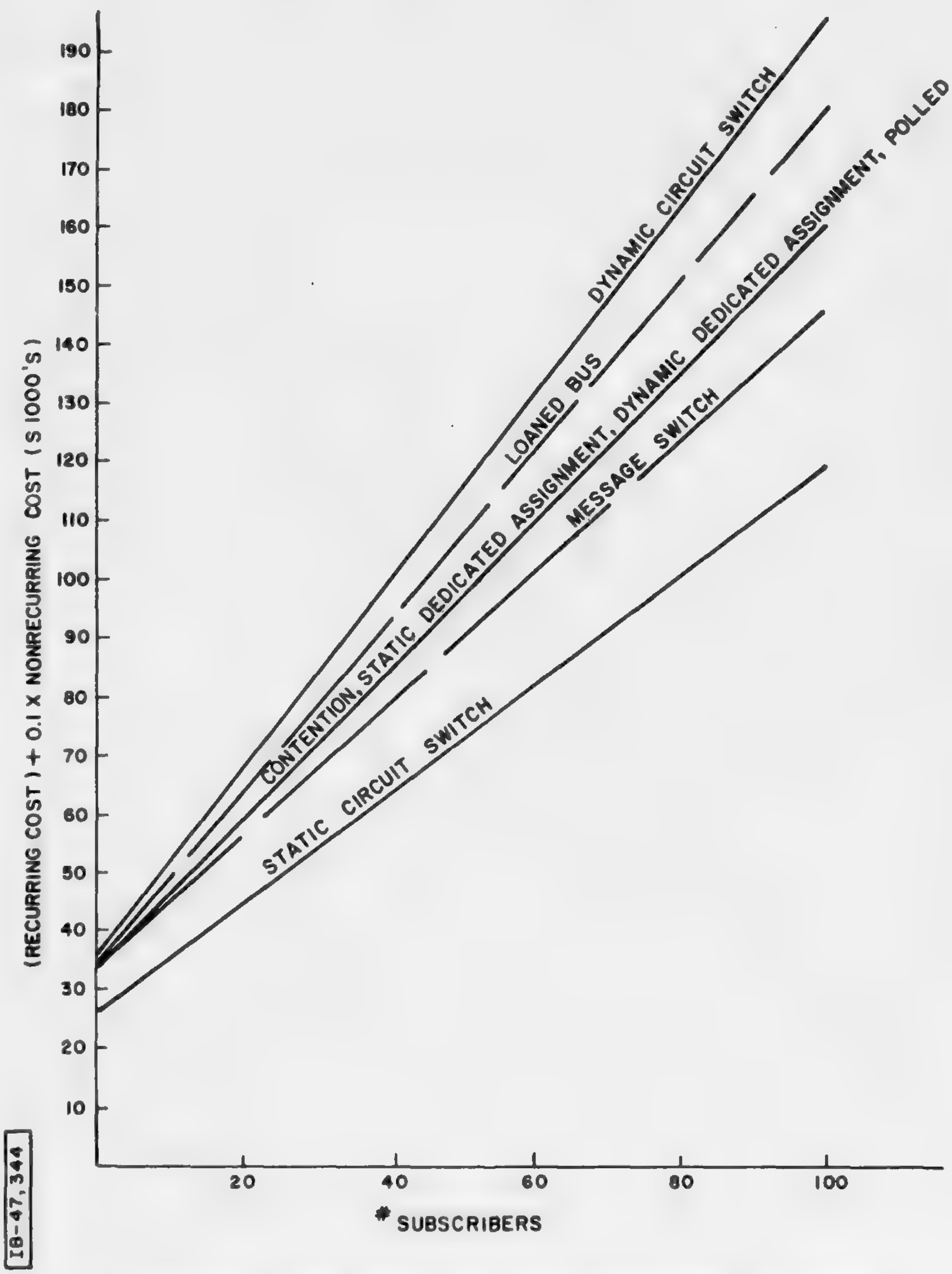

Figure 29. TOTAL COSTS FOR AN INTERCONNECT NETWORK
(NON-RECURRING COSTS SHARED AMONG 100 SYSTEMS)

SECTION V. RELIABILITY

INTRODUCTION

This section discusses the reliability of each of the eight interconnect alternatives being considered and summarizes the results of the analyses contained in Appendix B.

CONCLUSIONS

Table VI summarizes the results of the reliability analyses. The numbers shown in Table VI are the means of the high and low estimates for each alternative calculated in Appendix B. Two measures of reliability are presented. The first measure, system failure, is an indication of the mean-time-between-failure (MTBF) for any interconnect failure within the system and includes failures within the network control computer, data bus repeater, block-switching matrices, modems, etc. The estimates for major system components, have been found by statistically combining the MTBFs for the elements which comprise these devices. The MTBF for any system failure is determined by combining the component MTBFs. This procedure is discussed in Appendix B.

The second measure, single subscriber service MTBF, is an indication of the failure rate experienced by an individual subscriber on the interconnect system while he is exchanging data with another subscriber. Thus, it includes only that equipment which is involved directly in such a transfer. For example, the static circuit switch includes two subscriber interface units, cabling, and the block-switching matrix; the dynamic circuit switch includes the above items plus the control computer and multiplexer. The details of the calculations for all the alternatives are presented in Appendix B.

In general, the control computer is the least reliable element, with an MTBF of 1,000 to 10,000 hours. Therefore, the computer limits single subscriber service MTBF for the three systems where it is required: the dynamic circuit switch, the message switch, and the dynamic dedicated assignment bus. While the dynamic dedicated assignment bus has an MTBF for full operation which is determined by the network control computer, communications can be supported if that computer sustains a failure. However, the interconnect will be able to function only with the existing connectivity, i.e., as a static dedicated-slot bus. In the remaining bus alternatives, the least reliable element is the data bus repeater, with an MTBF of 18,000 to 213,000 hours.

TABLE VI

SYSTEM MTBF SUMMARY

	Static Ckt Switch	Dynamic Ckt Switch	Message Switch	Contention	Static Ded Assign	Dynamic Ded Assign	Polled	Loaned
SYSTEM FAILURE	736	677	2980	4050	4050	4050	4050	4050
SINGLE-SUBSCRIBER SERVICE FAILURE	36,800	4580	4682	34,000	34,000	4730*	4730	4730

*DEGRADED MODE AT 4730 Hrs MTBF
TOTAL FAILURE AT 34,000 Hrs MTBF

The main reliability limitations for the circuit switch interconnects are caused by the network control computer, multiplexer, and block-switching matrices. The network control computer is more complex for the dynamic circuit switch than for the static circuit switch. Consequently, the MTBF for the dynamic circuit switch is lower. Because of its large number of modems, one per subscriber, the block-switching matrix has a lower reliability than any element except the computer.

For the bus alternatives, other factors which affect reliability include the cable network and the possibility of a malfunctioning SIU. Since the cable is located in an enclosed environment, it is unlikely to be cut or physically damaged. Cable amplifiers are far less complex than the SIU and, therefore, have a much higher MTBF.

The malfunctioning SIU problem can be resolved by placing an energy sensing circuit on the output. If the unit transmits for a longer time period than is permitted by the bus protocol, the output is open circuited. This sensing device requires few semiconductor devices. Consequently, it has such a high MTBF that it does not affect the results of this analysis.

One method of improving the reliability is to add redundancy. Critical elements such as the network control computer and data bus repeater can be made redundant. If the primary unit fails, the secondary unit automatically becomes operational. As shown in Figure 1, this can substantially improve reliability.

APPENDIX A

DERIVATION OF PERFORMANCE RELATIONSHIPS

INTRODUCTION

Appendix A presents mathematical derivations for the performance relationships presented in Section III of this report.

CIRCUIT SWITCH

The relations for circuit switching systems were derived directly from graphs and formulas presented in Reference 5.

MESSAGE SWITCH

The message switch relationships presented in Section III were derived from the data in Reference 3 pertaining to telephone switching systems. This was accomplished by assuming a message switch processing time per message which was independent of the number of subscribers attached to the network and to the message length. Time spent in buffering was not included in the processing time. That is, the message processing time was taken to be the processing time required to transfer the message block from input to output buffers of the message switching computers and not the time spent by the message residing in one or the other buffer. Thus, the processing time translates directly into the service time, t_s, defined in Reference 1; the time for which the message resides in an input buffer translates into waiting time t_w, and the data presented for a circuit switch of capacity N = 1 applies.

CONTENTION BUS

In an unslotted contention network, subscribers share a common channel but transmit their data as if it were a dedicated channel. Subscribers transmit data without any central coordination. After the data has been transmitted, it will be acknowledged if it successfully enters the channel. Due to the unstructured nature of the system, it is possible for the messages from two or more subscribers to overlap. This is referred to as a contention. When a contention occurs, neither subscriber succeeds in transmitting. If a subscriber does not receive his own message relayed on the outbound lines within a specified time, the SIU retransmits the message with a random delay. The Abramson analysis (Reference 4) is extended by Metcalfe (Reference 5) as follows:

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Let:

α = message arrival rate for each subscriber

K = total number of subscribers

1/G = transmission rate for a subscriber given that the message has experienced contention

Q = the number of subscribers currently in the contention state (that is, transmitting at the rate 1/G)

m = the aggregate system message arrival rate

$\bar{b}$ = the average number of bits in a message

C = system capacity

Using the notation just defined, the aggregate message arrival rate, m, is seen to be:

$$m = (K-Q)\alpha + Q/G$$

This is true because Q of the subscribers will be in the process of retransmitting messages (at a rate equal to 1/G) and K-Q subscribers will be originating messages (at a rate equal to α). As an approximation, it will be assumed that when a new message arrives, it is delayed in the same way a retransmission is delayed. All messages are assumed to be transmitted at rate 1/G. Then, the aggregate transmission rate can be approximated as:

$$m \approx Q/G$$

The probability that a subscriber will experience contention is the probability that his message will overlap with a message from any of the Q-1 other terminals. This probability, P_c, is:

$$P_c = 1 - e^{-2((Q-1)/G)\bar{b}/C}$$

where: $\bar{b}/C$ is the average duration of a message.

In a steady-state, the rate at which new messages are originated, $(K-Q)\alpha$, is equal to the rate at which blocked messages are successfully transmitted, $m(1-P_c)$:

$$(K-Q)\alpha = \frac{Q}{G} \exp\left(\frac{-2(Q-1)\bar{b}}{GC}\right)$$

This traffic, m = Q/G, which supports the maximum throughput is found by maximizing the right side of the steady-state equation with respect to Q. This results in a transmission rate of $C/\bar{b}$ transmissions per second. Substituting this value for the transmission rate on the left side of the steady-state equation results in a throughput of 1/2 exp $(\frac{1}{Q} - 1)$ channel seconds per second. This is a decreasing function of Q. The throughput starts at 1/2 channel seconds per second. As the number of subscribers in the contention state increases, the throughput decreases to 1/2e channel seconds per second.

The maximum number of subscribers, K_{max}, which can use the system, is found from the steady-state relation:

$$(K_{max} - Q) = \frac{C}{\alpha 2\bar{b}} \quad e^{-2(Q-1)\bar{b}/CG}$$

$$K_{max} = \frac{C}{2\bar{b}\alpha} e^{-2(Q-1)\bar{b}/CG}$$

$$K_{max} = \frac{C}{2\bar{b}\alpha e} \left[G\alpha e + e^{2\bar{b}/GC}\right]$$

This shows that the maximum number of subscribers depends upon the average arrival rate for new messages, mean-time between retransmissions, number of bits in a message, and the system capacity. As expected, increases in the mean retransmission time result in longer delays.

Block time is the period during which the subscriber is retransmitting a message. If the delay between retries is exponentially distributed with mean G, the block time distribution is also an exponential distribution with mean $G/(1-P_c)$.

This does not lead to a concise expression for the capacity. However, the capacity can be found iteratively using the equation for the maximum number of subscribers.

The model for a slotted contention system is similar to that for an unslotted contention system. However, there are restrictions on the transmission of messages. The transmissions must occur in time units called slots. This decreases the bandwidth utilization efficiency, because it is likely that many of the slots will be only partly full.

Let:

α = the new message arrival rate

K = the number of subscribers

T = the slot duration in seconds

Since the messages are assumed to arrive randomly, the probability of n messages being transmitted in an interval T can be found from a Poisson distribution with parameter A, P(n arrivals in (t, t+T)) = $\frac{(AT)^n}{n!} e^{-AT}$. The parameter A is the message arrival rate. This includes both new messages and retransmissions. If P_c is defined to be the probability of contention, $A = K\alpha + AP_c$.

A contention occurs if two or more messages arrive in a time interval of length T. Therefore, the contention probability, P_c equals $1 - e^{-2AT}$. The arrival rate A, is seen to be equal to $A = K\alpha + A(1 - e^{-AT})$. This can be rearranged to yield:

$$K\alpha = Ae^{-AT}$$

The system throughput is the product of the service time, T, and the new message arrival rate K. This is seen to be:

$$K\alpha T = mTe^{-mT}$$

The maximum effective throughput is the product of the aggregate arrival rate, m, and the service time, T. This can be determined by maximizing $K\alpha T$ with respect to mT.

$$\frac{d(K\alpha T)}{d(mT)} = 0$$

$$AT = 1$$

Substitution of this value into the equation for system throughput results in:

$$K\alpha T = \frac{1}{e}$$

$$K = \frac{1}{e\alpha T}$$

The system capacity, C, equals $\bar{b}/T$.

Substituting for T:

$$K = \frac{C}{e\alpha\bar{b}}$$

This analysis indicates that the slotted system can support about twice as many users as the unslotted contention system (Reference 6).

One of the drawbacks of this model is that it assumes an infinite number of subscribers. A more detailed model which shows a finite number of subscribers follows. This model developed by Metcalfe (Reference 5), yields a gradual degeneration as more subscribers enter the system.

In addition to the variables defined for the unslotted contention case, the following are required for a slotted contention model:

T = slot duration

X = probability of transmission given a ready message

W = the probability that a slot has exactly one message in it

Using the binomial distribution, W can be expressed as:

$$W = Q(X(1-X)^{Q-1})$$

W/T is the channel throughput. During steady-state, an equal number of subscribers submit messages and transmit successfully.

$$(K-Q)\alpha = \frac{W}{T}$$

Substituting for W:

$$(K-Q)\alpha = \frac{Q}{T}(X(1-X)^{Q-1})$$

Solving for K:

$$K = Q + \frac{Q}{T\alpha} \left(X(1-X)^{Q-1}\right)$$

This is the number of subscribers that can use the system.

The block time for a slotted contention system can be found as a function of the probability of a successful transmission, W. The probability that a specific subscriber will attempt and succeed with a transmission is W/Q. The probability that the Sth slot following the message generation contains the message is $(W/Q)(1-W/Q)^{S-1}$. The mean delay can be found using the following summation:

$$\text{Delay} = \sum_{S=1}^{\infty} \frac{STW}{Q} \left(1-\frac{W}{Q}\right)^{S-1}$$

This yields $\frac{TQ}{W}$. Since the messages arrive uniformily within the slots, the total mean delay is $\frac{T}{2} + \frac{TQ}{W}$.

STATIC DEDICATED ASSIGNMENT BUS

In a static bus, each subscriber is given a fixed, unique slot assignment in which to transmit data. The number of slots per frame assigned to a subscriber is determined by the data rate required and the response time required. For this Appendix, it will be assumed that a slot contains 256 data bits and 128 overhead bits. For a frame period of 0.85 seconds, this leads to a data rate of 300 bps for a one slot per frame assignment.

Assume that each subscriber has an arrival rate of α messages per second. Further, assume that the average message length is $\bar{b}$ bits. (This is the same assumption used for the polled network.) The average subscriber will require a data rate of $\bar{b}\alpha$ bits per second. If the frame length is 0.85 second, then the number of bits per frame required by the average subscriber is $0.85\ \bar{b}\alpha$. The minimum number of slots required for the average subscriber is $0.85\ \bar{b}\alpha/256$ since each slot has 256 data bits. However, the slot assignments must contain an integer power of two number of slots per frame. So the total number of slots per frame required by the average subscriber for data transmission is the smallest power of two which is greater than or equal to $0.85\ \bar{b}\alpha/256$. This number is defined to be $S(0.85\ \bar{b}\alpha/256)$. If there are K subscribers in the system, the minimum number of slots per frame required to transfer data from terminals is $KS(0.85\ \bar{b}\alpha/256)$. An additional 10%

of this allocation must be provided for the computer. Therefore, define $\dot{K} = 1.1K$. The 10% computer allocation is discussed in Appendix C.

The total number of slots in a frame must be an integer power of two. Consequently, the number of slots per frame is equal to the smallest power of two greater than $\dot{K}S(0.85\ \bar{b}\alpha/256)$ which is equal to $S(\dot{K}S(0.85\ \bar{b}\alpha/256))$.

A numerical example will clarify the expressions which were just derived. If the average message length, $\bar{b}$, is 1,000 bits, and the arrival rate α, is one message per second, then the average data rate required is 1,000 bits per second. This translates to 850 bits per frame since the frame is 0.85 seconds long. This means that the average subscriber transfers 850 bits of data in each frame. A slot is 384 bits long, but contains only 256 data bits. So, a total of 850/256 = 3.3 slots per frame are required to transfer the 850 bits. The slot assignment becomes S(3.3) = 4 slots per frame. This is actually a data rate of 1,200 bits per second, however, the additional capacity is required to meet system requirements. If there are 2,500 subscribers, the number of slots per frame must exceed 2,500 X 4 X 1.1 = 11,100. The smallest power of two greater than 11,100 is 16,384. Therefore, there are 16,384 slots per frame.

These results can be used to determine the response time and system capacity. Slots in assignments are evenly spaced in the frame. If a subscriber has 4 slots per frame, the interval period between its slots is .85/4 = .21 seconds. If the message arrivals are uniformly distributed, this gives the average subscriber a $\frac{.21}{2} \approx .1$ second access time. If a shorter time is required, the subscriber can be given a larger assignment. This results in a trade-off between access time and bandwidth utilization. If there is a requirement that the average access time be on the order of .05 seconds, each subscriber must have an assignment of 8 slots. Using the same number of subscribers, 2,500, the new value for the number of slots required to transfer data is 20,000. The total number of slots per frame would be 32,768.

The system capacity is found by dividing the total number of bits per frame by the frame period. Since there are 16,384 slots, each containing 384 bits, the number of bits in a frame is 6,291,456. With a frame period of .85 seconds, the capacity is 7.37 Mbps. Recall that only two thirds of this can be used for data and that an even smaller fraction is actually used for data transfer.

These results may be restated in a more succinct form:

$\bar{b}$ = average number of bits per message

α = average arrival rate (messages/second)

K = number of subscribers

$S(.)$ = the smallest integer power of two which is greater than the argument

d = number of data bits per slot

b' = number of overhead bits per slot

f = frame period

$\bar{b}\alpha$ = average number of bits per second required per subscriber

$\bar{b}\alpha f$ = average number of bits per frame required per subscriber

$\frac{\bar{b}\alpha f}{d}$ = average number of slots per frame required to transfer subscriber data

$S(\frac{\bar{b}\alpha f}{d})$ = number of slots per frame assigned to the average subscriber

$K'S(\frac{\bar{b}\alpha f}{d})$ = number of slots per frame required to form subscriber assignments and computer assignment

$S(K'S(\frac{\bar{b}\alpha f}{d})$ = $S(K')S(\frac{\bar{b}\alpha f}{d})$ = total number of slots required per frame

$\frac{f}{2S(\frac{\bar{b}\alpha f}{d})}$ = average access delay

$\frac{S(K)S(\frac{\bar{b}\alpha f}{d})(d+b')}{f}$ = bandwidth required

POLLED BUS

In a polled system, a central control device successively issues polls to each subscriber. If the subscriber has a message ready, it responds to the poll by transmitting the message. Otherwise, the subscriber returns a standard null response.

To determine the bandwidth requirements and the response times for this type of system, it is necessary to define a set of variables:

α = message arrival rate for each subscriber

b = random variable equal to the number of bits in a message (including overhead)

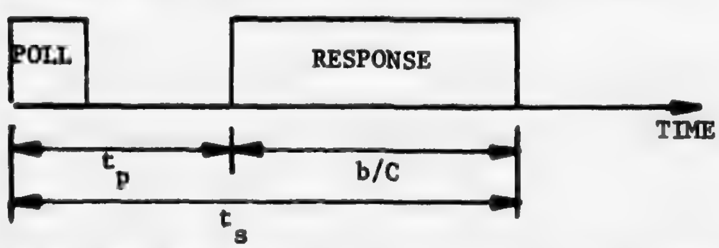
K = number of subscribers on the network

t_p = time required to issue a poll

C = network capacity

t_s = total time required to service a subscriber

Some variables are related in the following diagram:



t_p includes the processing time required by the computer and all propagation delays. b/C is the time required to transfer b bits at a rate of C bits per second. If the subscriber does not have a message ready, then b is very small. In this case, the subscriber replies with a short standard response. If the subscriber does have a message, b is equal to the total number of bits in the message. t_s is the total duration of the polling cycle. Strictly speaking, t_s is a random variable which depends upon the number of bits in the subscriber's message. To simplify the analysis, t_s is assumed to be a constant which is determined by the mean value of b, $\bar{b}$. Thus,

$$t_s = t_p + \bar{b}/C$$

This approximation greatly simplifies the results. It will yield a good estimate of response times provided that the variance of b is much less than $\bar{b}$. For this analysis, t_s is the average time required to service a single subscriber.

Each subscriber issues an average of α messages per second. Since there are K subscribers, the total system demand is $K\alpha$ messages per second. The average length of these messages is $\bar{b}$ bits. $1/K\alpha$ is the average time interval between message arrivals. Therefore, to avoid unstable queues, the mean service time must be less than or equal to the mean interarrival time. This may be expressed as follows:

$$t_s = t_p + \bar{b}/C \leq 1/K\alpha$$

This relation may be solved for C:

$$C = \frac{K\alpha\bar{b}}{1-K\alpha t_p}$$

If $C \geq \frac{K\alpha\bar{b}}{1-K\alpha t_p}$, the queue length at each subscriber is zero. This follows naturally from the fact that each subscriber will be polled on the order of every $1/\alpha$ seconds and will have a message available every $1/\alpha$ seconds.

LOANED BUS

A loaned bus is similar to a polled bus. The system is capable of handling only one subscriber at a time. However, rather than successively poll each subscriber, the network control center receives requests from the subscribers and queues them. This type of protocol is preferable to a polling system only when a small percentage of the subscribers will want to transmit during an interval because the overhead associated with polling inactive terminals is eliminated. Conversely, if the load is fairly constant, polling is a better choice.

The loaned bus may be slotted or unslotted. This analysis assumes the unslotted case. The requests are sent spontaneously by subscribers to the network control center and an acknowledgement is sent by the control center to the subscriber. When the network is available, the control center informs the subscriber that it can use the system. At the end of the transfer, the system is allocated to another subscriber.

The areas of interest for this analysis are: the time required to get a request to the network control center (Access Time), the queue time at the network control center, and the capacity required.

Access Time

A simple model of the access time will be presented here. It is based on Abramson's (Reference 4) analysis of the ALOHA System. A more sophisticated model is discussed in the section on contention systems. Essentially, the access to a loaned bus is a contention system. However, the request messages are short so the contention problem disappears. In the discussion of contention systems, the messages are longer so more conflicts will occur.

Let:

α = the message arrival rate

K = the number of subscribers

m = the number of bits in the request message

C = capacity allocated to requests

Then:

$$\frac{m}{C} = T = \text{the duration of a request}$$

If the messages arrive randomly, then the probably of two or more requests interfering with each other is:

$$P_c = 1 - e^{-2K\alpha T}$$

Now assume that the subscribers automatically retransmit their requests if no acknowledgement is received after a random wait. This means that the effective arrival rate is greater than α because some requests will be repeated. If the effective arrival rate is labeled A, the conflict probability becomes:

$$P_c = 1 - e^{-2AT}$$

and A is defined as:

$$A = K\alpha + AP_c$$

$$A = K\alpha + A(1 - e^{-2AT})$$

rearranging:

$$K\alpha = Ae^{-2AT}$$

A measure of the throughput of the system is $K\alpha T = ATe^{-2AT}$. To maximize the effective throughput, $K\alpha T$ is differentiated with respect to AT and the result is set equal to zero.

$$\frac{d(K\alpha T)}{d\ AT} = e^{-2AT} - 2ATe^{-2AT} = 0$$

$$1 - 2AT = 0$$

$$AT = 1/2$$

Substituting this value for AT into the expression for $K\alpha T$ yields:

$$K\alpha T = \frac{1}{2e}$$

$$K = \frac{2}{2e\alpha T}$$

$$K = \frac{C}{2e\alpha m}$$

This equation provides a method of determining the maximum number of subscribers which can be on the system for a given bandwidth before the requests begin to develop a serious contention problem. In general, the request contention issue will be neglected and the access time will be lumped together with processing and propagation delay times.

Queue Delay and System Capacity

The queue delay is determined by the arrival and service rates. The message arrival rate is α. The service time is equal to t_s (the lumped access time, switching time, etc.) plus the time required to transmit the data, $\bar{b}/C$. If $1/\sigma$ is the service time, then it may be expressed as:

$$1/\sigma = t_s + \bar{b}/C$$

Note that this is the same form as the equivalent equation for a polled network.

A measure of throughput can now be defined as:

$$f = \frac{\alpha}{\sigma}$$

If $\int > 1$ then messages arrive faster than they can be serviced and unstable queues develop. However, if $\int \leq 1$ the queue will remain finite. $\int$ is the ratio of the mean service time to the mean inter-arrival time of messages. The probability of a queue of length n is:

$$P_n = \int^{n-1} (1-\int)$$

The average delay (analogous to the delay derived for the polled network) is:

$$\text{Average Delay} = \sum_{n=o}^{\infty} \left(\frac{n}{\sigma}\right) P_n$$

However, with this model, the probability of any specific delay is also obtainable. Since σ depends upon the system capacity, this provides a method of finding the probability that a subscriber will experience a specific delay for a given system capacity.

SUMMARY

The expressions for capacity and response time developed for the various interconnect approaches, are summarized in Table VII.

TABLE VII

	CAPACITY RELATIONSHIP	DELAY RELATIONSHIP
CIRCUIT SWITCH	$N_c \geq (t_d+\bar{b}/C)\alpha K$	$\bar{t}_w = \frac{(t_d+\bar{b}/C)\alpha K}{N_c-(t_d+\bar{b}/C)\alpha K}$
MESSAGE SWITCH	$N_m \geq t_s \alpha K$	$\bar{t}_w = \frac{t_s}{N_m - t_s \alpha K}$
POLLED BUS	$C \geq \frac{K\alpha\bar{b}}{1-\alpha t_p}$	0 for $C > \frac{K\alpha\bar{b}}{1-K\alpha t_p}$
LOANED BUS	$C = \frac{\bar{b}}{\bar{b}-t_s}$	$\sum_{n=1}^{\infty} (\frac{n}{\sigma}) (\frac{\alpha}{\sigma})^n (1-\frac{\alpha}{\sigma})$
UNSLOTTED CONTENTION	$C = 2e\alpha\bar{b}K$	$\sum_{n=1}^{\infty} P_c^{\,n-1}(n-1)(\text{mean interarrival time})(1-P_c)$
SLOTTED CONTENTION	$C = e\alpha\bar{b}K$	$\sum_{n=1}^{\infty} P_c^{\,n-1}(n-1)(\text{mean interarrival time})(1-P_c)$
STATIC DEDICATED ASSIGNMENT	$C = \frac{S(K)S(\frac{\bar{b}\alpha f}{d})(d+b')}{f}$	$\frac{f}{S(\frac{\bar{b}\alpha f}{d})}$

DEFINITION OF TERMS IN SUMMARY TABLE

α	=	average message arrival rate per subscriber (messages/second)
$\bar{b}$	=	mean message length (bits)
b'	=	number of overhead bits per slot
C	=	capacity (bits per second)
d	=	number of data bits per slot
F	=	frame length (seconds)
K	=	number of subscribers
N_c	=	number of switching channels required
N_M	=	number of parallel message switches required
P_c	=	probability of contention
$S(\cdot)$	=	smallest integer power of two which is greater than the argument
t_d	=	switch dwell time (seconds)
t_p	=	overhead time associated with poll (seconds)
t_s	=	processing delay per message in computer excluding buffering (seconds)
$\bar{t}_w$	=	average waiting time (seconds)
$1/\sigma$	=	message service rate (messages/second)

APPENDIX B

RELIABILITY ANALYSIS

Appendix B presents details of the reliability estimates for the various alternatives.

The reliability of the SIUs, block-switching matrices, and data bus repeater were calculated using estimated component counts for these elements derived from prototype design and fabrication efforts conducted by MITRE. Reliability figures for various classes of components were estimated on the basis of past experience with similar devices as well as from the manufacturers' specifications and specific data included in the RADC Reliability Notebook (Reference 7). The reliability figures used are shown in Table VIII. The component count and resulting system element reliabilities are shown in Table IX.

The figures shown for the computer are based upon manufacturers' data. The cable distribution network is omitted from the calculations because experience in the CATV industry has shown it to be far more reliable than other elements of the system. The reliability calculations are made using the standard formula:

$$\text{MTBF (system)} = \frac{1}{\sum \frac{1}{\text{MTBF (components)}}}$$

The system failure rates are calculated by aggregating the system component failure rates, as shown in Table X. The calculations are based upon a system with 100 subscribers.

These failure rates are calculated in a similar fashion, but only those elements which are connected in series are included in the computation.

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TABLE VIII

ASSUMED RELIABILITY FIGURES

COMPONENT	ASSUMED MTBF (Hours)	
	LOW	HIGH
Transistors	2.5×10^6	2.5×10^7
Medium Scale and Small Scale Integrated Circuits	1×10^7	2×10^8
Large Scale Integrated Circuits	5×10^6	1×10^8
Power Supply	3×10^4	3×10^5

TABLE IX

SYSTEM ELEMENT RELIABILITIES

SYSTEM ELEMENTS	COMPONENT COUNT				SYSTEM ELEMENT MTBF (Hours)	
	Transistors	MSI Circuits	LSI Circuits	Power Supply	Low	High
SIU - Static Circuit Switch (Modem & I/O Module)	20	39	6	1	22,000	186,000
SIU - Dynamic Circuit Switch (Modem, I/O, & Logic Module)	20	84	30	1	21,000	171,000
SIU - Message Switch (Modem & I/O Module)	20	39	6	1	22,000	186,000
SIU - All Bus Options (Modem, I/O,& Logic Module)	20	84	30	1	21,000	171,000
DBR	20	75	24	1	18,000	212,000
Block Switching Matrix - System Reliability (128 modems, and 60 switching circuits)	2560	3968	60	1	1,800	7,900
Block Switching Matrix - Single Subscriber Service Reliability (2 modems and 4 switching circuits)	40	60	4	1	17,000	234,000
Control Computer		Based on Manufacturer Data			1,000	10,000
Multiplexer - System Reliability (128 ports)	0	1152	768	1	3,300	56.500
Multiplexer - Single Subscriber Service Reliability (2 ports)		18	12	1	6,000	222,000
Cable System					Very High	Very High

TABLE X

SYSTEM RELIABILITY ESTIMATES

ALTERNATIVE	SYSTEM ELEMENT	SYSTEM RELIABILITY		SINGLE SUBSCRIBER SERVICE RELIABILITY	
		QUANTITY OF ELEMENTS	MTBF (SYSTEM)	QUANTITY OF ELEMENTS	MTBF (SINGLE SUBSCRIBER)
Static Circuit Switch	SIU Blockswitching Matrix Computer	100 1 1	162 → 1310	2 1 0	6758 → 66,700
Dynamic Circuit Switch	SIU Blockswitching Matrix Multiplexer Computer	100 1 1 1	150 → 1205	2 1 1 1	867 → 8300
Message Switch	SIU Multiplexer Computer	100 1 1	1690 → 4270	2 1 1	795 → 8600
Contention Bus	SIU DBR Computer	100 1 1	1770 → 6320	2 1 0	6890 → 61,000
Static Dedicated Assign. Bus	SIU DBR Computer	100 1 1	1770 → 6320	2 1 0	6870 → 61,000
Dynamic Dedicated Assign. Bus	SIU DBR Computer	100 1 1	1770 → 6320	2 1 1	873 → 8591
Polled & Loaned Bus	SIU DBR Computer	100 1 1	1770 → 6320	2 1 1	873 → 8591

APPENDIX C

COMPUTER SLOT ALLOCATION

Appendix C discusses the dedicated slot allocation required by a computer which serves many terminals.

The capacity required is less than the total capacity required for all the terminals being served. For example, 100 terminals at 9600 bits per second each do not require 9600 X 100 = 960,000 bits per second of slot assignment be made to the computer. In fact, the slot assignment which is required depends upon the duty cycle of the various terminals involved and upon the probable queuing delay for messages from the computer onto the communications bus.

An expression in terms of terminal receive duty cycle, slot length on the bus, and mean message length is given below with the assumption that messages have exponentially distributed length. While constant message length implies a slightly lower capacity requirement, a closed form expression for this case has not been attempted since the exponentially-distributed form yields conservative results (see Reference 4).

$$\frac{t_w}{t_m} = \frac{1}{N-A}$$

where:

t_w = mean wait time for a given message to be transmitted on the bus

t_m = mean transmission time on the bus of an entire message at the subscriber terminal data rate

N = the bit rate assigned to the computer (that is, for the case of 9600 bit per second terminals cited above, 960,000 bits per second would correspond to N = (100))

A = message traffic density of replies to all terminals, in Erlangs.

The value of A may be expressed as follows:

$$A = \eta \delta T$$

where:

T = the number of subscriber terminals in the system

δ = the average duty cycle of such a terminal

η = the slot efficiency per message, as derived in Appendix A.

Therefore,

$$N = \frac{t_m}{t_w} + \eta\delta T$$

This expression for N is shown graphically in Figure 30 for a mean message length of 10,000 bits and for $(t_m/t_w) = 10$. This message length is considered plausible since the majority of terminal devices are likely to frequently request full page displays. The value of t_m/t_w implies a 10% addition to each terminal's wait time to obtain a complete message; this is judged to be insignificant to the user.

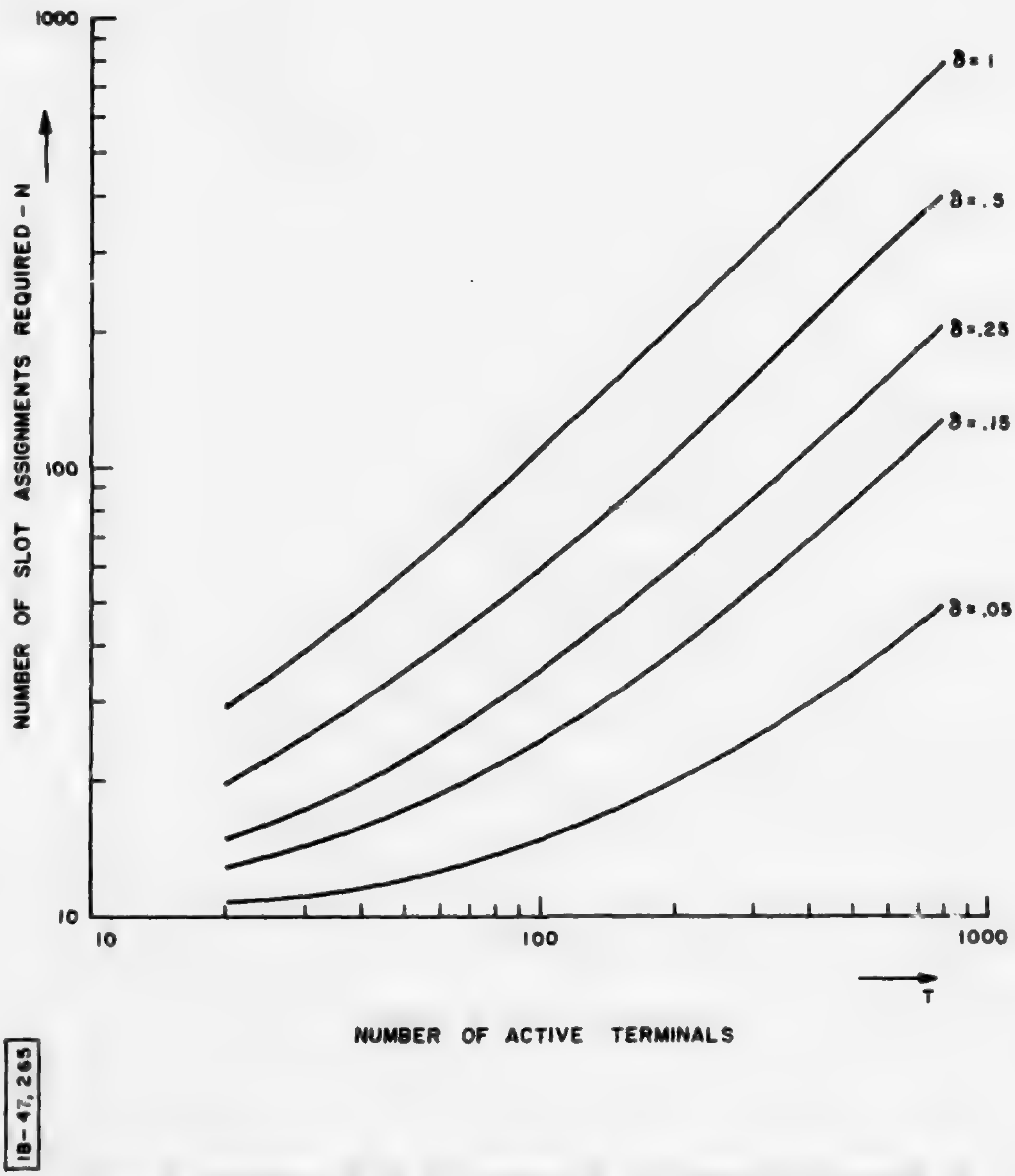

Figure 30. COMPUTER SLOT ALLOCATION AS A FUNCTION OF NUMBER OF ACTIVE USERS FOR $\frac{t_w}{t_M} \leq 0.1$; 10^4 BITS PER MESSAGE

APPENDIX D

ANNOTATED BIBLIOGRAPHY

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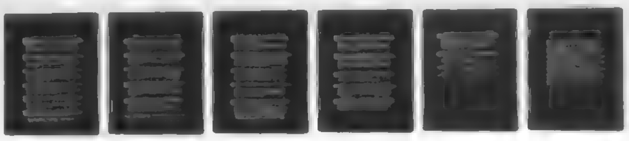

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